Interconnect (1)

Lecture 8
18-322 Fall 2003

Textbook: [4.1-4.4.5]

[Slides on RC Trees and Elmore delay model adapted from R. Rutenbar, 18-760 “Logic To Layout”, CMU Fall 2001]

Overview

- Interconnect parameters
  - Capacitance
  - Resistance
    - Inductance (much later in the sequel)

- Electrical wire models
  - Lumped RC model
  - Elmore delay
Transistors Everywhere…

- Node-centric perspective
  - Focus on devices and their properties
- Network-centric perspective
  - Focus on interconnects (today)

Impact of Interconnect Parasitics

- Reduce Reliability
- Affect Performance

Classes of Parasitics

- Capacitive
- Resistive
- Inductive
Why Does This Matter?

- **Problem**
  - Delays on signals due to wires are no longer negligible
  - Modern designs must meet tight timing specifications

- **Delay modeling**
  - **Sources for delay**
    - Delay comes from parasitic loading of the interconnect
    - Depends critically on the exact shape of the wired net
  - **Accurate prediction**
    - We’ll use a first-order model

INTERCONNECT

Dealing with Capacitance
Capacitance: The Parallel-Plate Model

\[ C = \frac{\varepsilon_{\text{ox}} WL}{t_{\text{ox}}} = C_{\text{ox}} WL \]

\[ \varepsilon_{\text{ox}} = \varepsilon_r \varepsilon_0 \text{ [F/m]} \]

- \( \varepsilon_r = \) dielectric constant (relative permittivity) = 3.9
- \( \varepsilon_0 = \) permittivity of the free space = 8.854 \( \times 10^{-12} \) [F/m]
- \( \varepsilon_{\text{ox}} = 3.5 \times 10^{-11} \) [F/m]

The Unit Transistor Capacitance

\[ C_g = C_{\text{ox}} WL \]

\[ t_{\text{ox}} = (100 - 200) \times 10^{-10} \text{ [m]} \]
\[ \lambda = 0.5 \mu m; \]
\[ W = 2 \mu m, L = 1 \mu m \]

\[ C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} = \frac{3.9 \times 8.854 \times 10^{-12}}{(100 - 200) \times 10^{-10}} = (35 - 17) \times 10^{-4} \text{ [pF/\mu m^2]} \]

\[ C_g = 2 \times 25.5 \times 10^{-4} \approx 0.005 \text{ [pF]} = 5 \text{ [fF]} \]
**Fringing Capacitance**

- In modern technologies $W/H$ is reduced $\rightarrow$ the parallel-plate model becomes inaccurate.
- The capacitance between the side-walls of the wires and substrate (fringing capacitance) becomes important.

**Interwire Capacitance**

Creates Cross-talk
Impact of Interwire Capacitance

![Graph showing impact of interwire capacitance](from [Bakoglu89])

**Capacitance Design Date**

- **From 0.25 micron**
- **Bottom Plate**

<table>
<thead>
<tr>
<th></th>
<th>Field</th>
<th>Active</th>
<th>Poly</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
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<tr>
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<td>M2 (pp)</td>
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<tr>
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<td>M3 (pp)</td>
<td>8.9</td>
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<td>10</td>
<td>15</td>
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<td></td>
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<td>7</td>
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<td>15</td>
<td>35</td>
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<td>18</td>
<td>27</td>
<td>45</td>
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<td>5.4</td>
<td>5.4</td>
<td>6.6</td>
<td>9.1</td>
<td>14</td>
<td>38</td>
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<td>12</td>
<td>12</td>
<td>14</td>
<td>19</td>
<td>27</td>
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</table>

Parallel Plate (pp) is in aF/µm²
- Fringe is in aF/µm
Inter-wire Capacitance per unit wire length

- For 0.25 micron wires, minimally spaced

<table>
<thead>
<tr>
<th>Fringe Capacitance</th>
<th>Poly</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
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<td>40</td>
<td>95</td>
<td>85</td>
<td>85</td>
<td>115</td>
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INTERCONNECT

Dealing with Resistance
Wire Resistance

\[ R = \frac{\rho L}{H W} \]

Sheet Resistance \( R_0 \)

\[ R_1 = R_2 \]

Ohms Per Square

Six Squares

Three Squares
Resistance of Non-rectangular Regions

Approximations derived from solving Poisson’s equation!

\[ \frac{W_1}{W_2} = 1 \]
\[ (L/W)_{eq} = 2.56 \]
\[ = (1\text{sq} + 1\text{sq} + 0.56\text{sq}) \]

\[ \frac{W_2}{W_1} = 1 \]
\[ (L/W)_{eq} = 2.2 \]

Example

Given:
\[ R = 40 \text{ m}\Omega/\square \]
\[ C_{\text{fringe}} = 0.044 \text{ fF/\mu m} \]
\[ C_{\text{plate}} = 0.031 \text{ fF/\mu m}^2 \]

Determine:
the resistance between A and B, the plate and fringe capacitances to ground.

\[ R = (9 + 2 \times 0.56 \text{ squares}) \times 40 \text{ m}\Omega/\square = 404.8 \text{ m}\Omega \]
\[ C_{\text{fringe,\ g}} = \text{Perimeter } C_{\text{fringe}} = 96.8 \text{ fF} \]
(Perimeter = 2200 \text{ \mu m})
\[ C_{\text{plate,\ g}} = \text{Area } C_{\text{plate}} = 3.41 \text{ pF} \]
(Area = 110,000 \text{ \mu m}^2)
Overview

- Interconnect parameters
  - Capacitance
  - Resistance

- Electrical wire models
  - Lumped RC model
  - Elmore delay
The Lumped Model

\[ V_{\text{out}}(t) = V_{\text{in}}(1 - e^{-t/\tau}) \text{ where } \tau = R_{\text{driver}} \times C_L \]

But, the wire isn’t ideal, it has resistance…

The Elmore Delay

\[ \tau_N = \sum_{i=1}^{N} R_i \sum_{j=1}^{i-1} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i-1} R_j \]
Lumped $\pi$ Network

$$V_{in} \rightarrow R \rightarrow C \rightarrow R \rightarrow \cdots \rightarrow \frac{1}{2}C_{line}$$

$$R = \frac{R_{line}}{N} \quad C = \frac{C_{line}}{N}$$

$$t_n = \frac{N(N+1)}{2} \quad t_{\infty} = \frac{1}{2} \left( \frac{R_{line}C_{line}}{2} \right)$$

This is the $\pi$ model!

RC Trees

Note: each of the Rs, Cs in this tree are probably different numbers, since each depends on the geometry of the segment.
Summary: Gates + Wires -> RC Trees

RC Trees: The Elmore Delay

- $\tau$ is "the Elmore delay"
- $\tau = \sum C_k R_k$

Assume one time constant $\tau$ is a good approximation for the actual delay
The Elmore Delay with RC Trees

\[ \tau_{D_I} = \sum_{k=1}^{N} C_k R_{ik} \]

Shared resistance among paths from root to nodes k and i

\[ R_{ik} = \sum \hat{R}_j \quad (\hat{R}_j \in \{ \text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k) \}) \]

Elmore Example

\[ R_0 = 20 \]

\[ \begin{align*}
W & = 1 \\
L & = 20 \\
\end{align*} \]

\[ \begin{align*}
W & = 1 \\
L & = 5 \\
\end{align*} \]

\[ \begin{align*}
W & = 1 \\
L & = 2 \\
C_L & = 1 \\
\end{align*} \]

\[ R = r \frac{L}{W} \]

\[ C = c (WL) \]

Assume: \( r = 1 \) \( c = 2 \)

Note: Since it is symmetric, we need to compute only one path!
Another Elmore Example

R₀ = 20
W = 1  L = 20
W = 1  L = 5
W = 1  L = 2
Cᵢ = 1

Another Elmore Example

Rᵢ = 20
W = 1  L = 20
W = 1  L = 5
W = 1  L = 10
Cᵢ = 1

R smaller
C bigger

R = 20
L = 5
C = 1

R = 20
L = 10
C = 1

T_left (5681)
T_right (7606)
Elmore Applications

- Elmore delay is the easiest to compute delay estimator
- Fairly accurate for symmetric designs
- Inaccurate for anything else
- Can be used for layout optimization (e.g. clock trees)
- For more accuracy, there are more sophisticated models