Layout Design

Lecture 4

18-322 Fall 2003

Textbook: Design Methodology Insert A

[Portions adapted from J. P. Uyemura "*Introduction to VLSI Circuits and Systems*", Wiley 2001.]

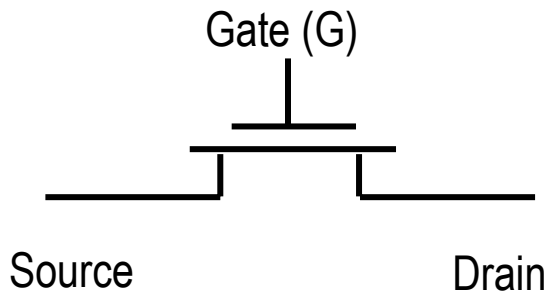
Roadmap

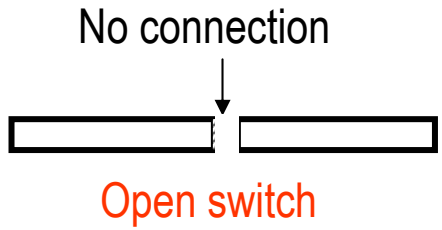
- Today: Basic CMOS Layout: “design in the small”
- Thursday: Layout Verification & “design in the large”
- Next week:
  - Transistor sizing
  - Wires
- Homework 1: Due Thursday
- Homework 2: Out Thursday
- Lab 2: This week

Today's Overview

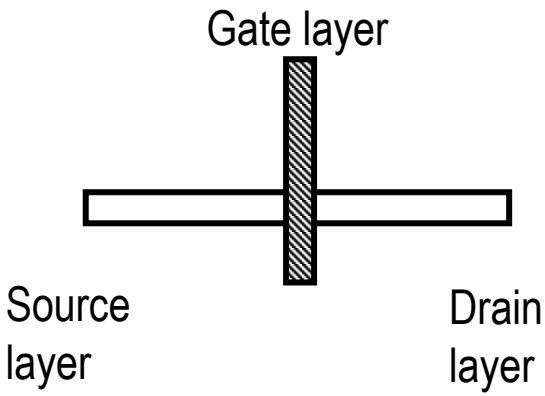
- Physical structure of ICs
  - Design rules
  - Basic gates layout
- Stick diagrams
  - Basic rules
  - Examples
- Cadence (Virtuoso)

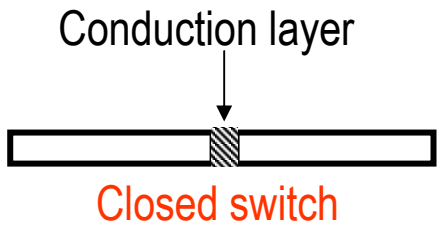
Review: MOSFETs





G = 0

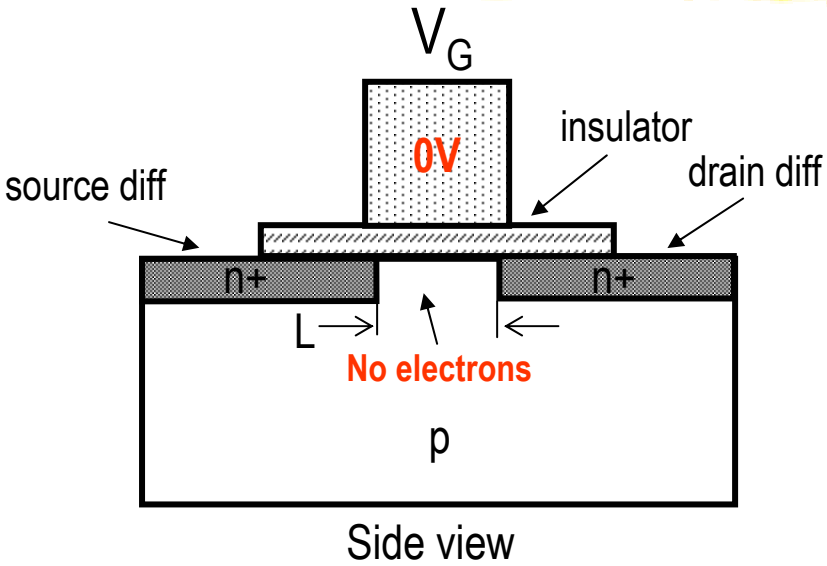


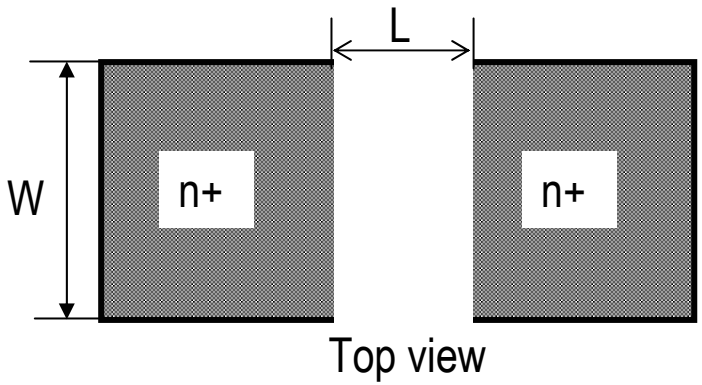


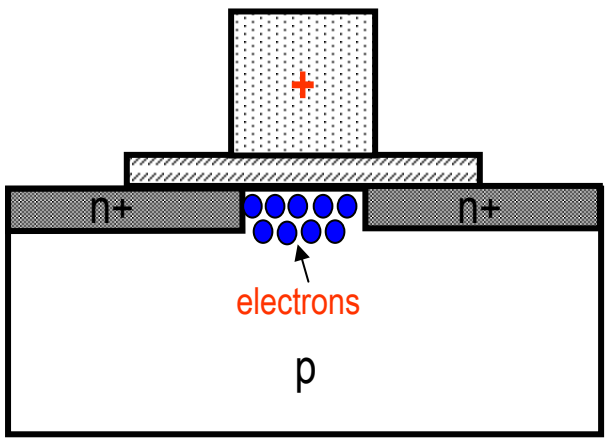
G = 1

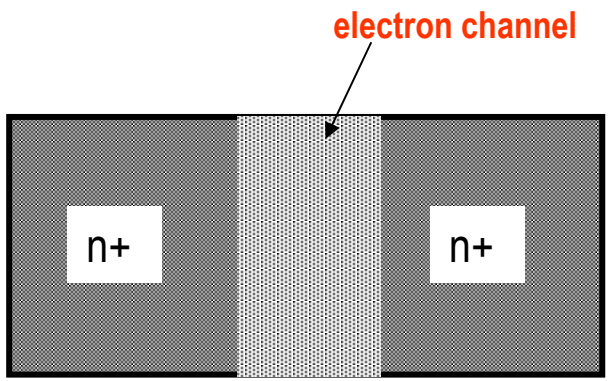
G is responsible for the absence or presence of the conduction region between the drain and the source regions

Review: Controlling Current Flow (nFET)

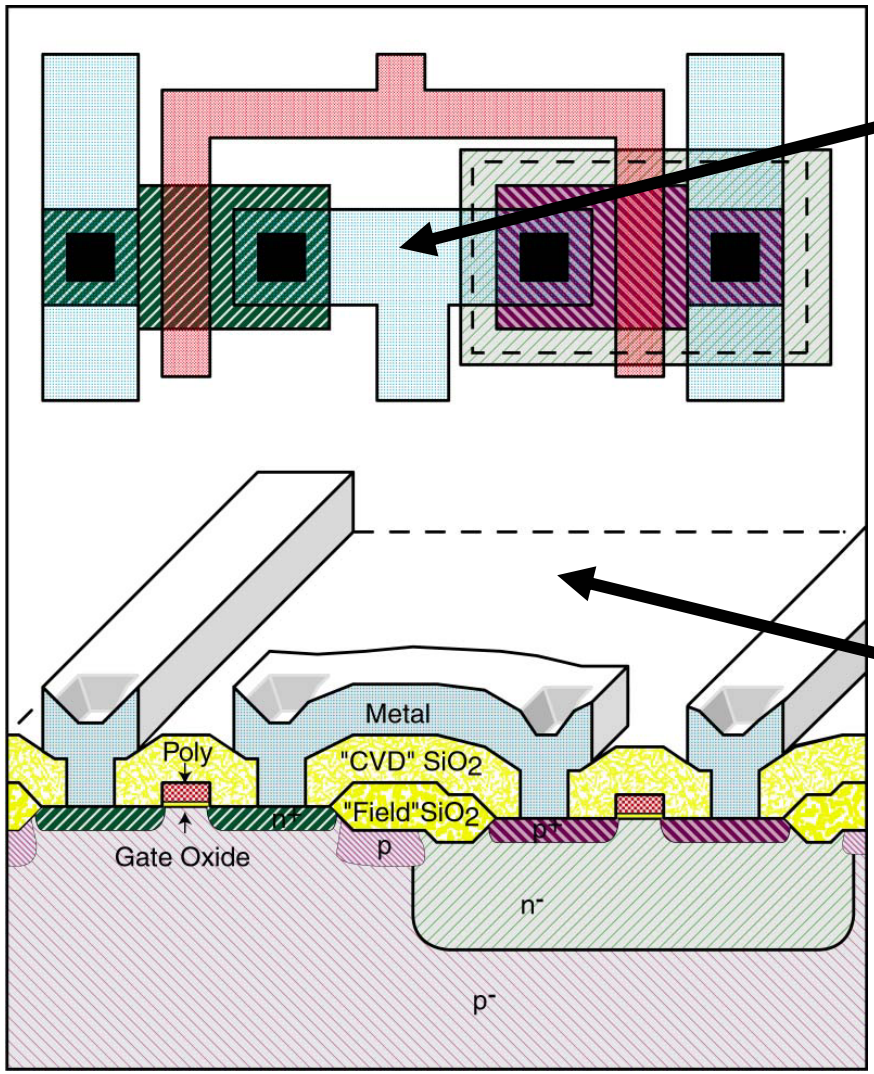








Review: Manufacturing



2D top-down view

How design engineers see the chip.

3D “cross-section” view

How process engineers see the chip.

Design Rules

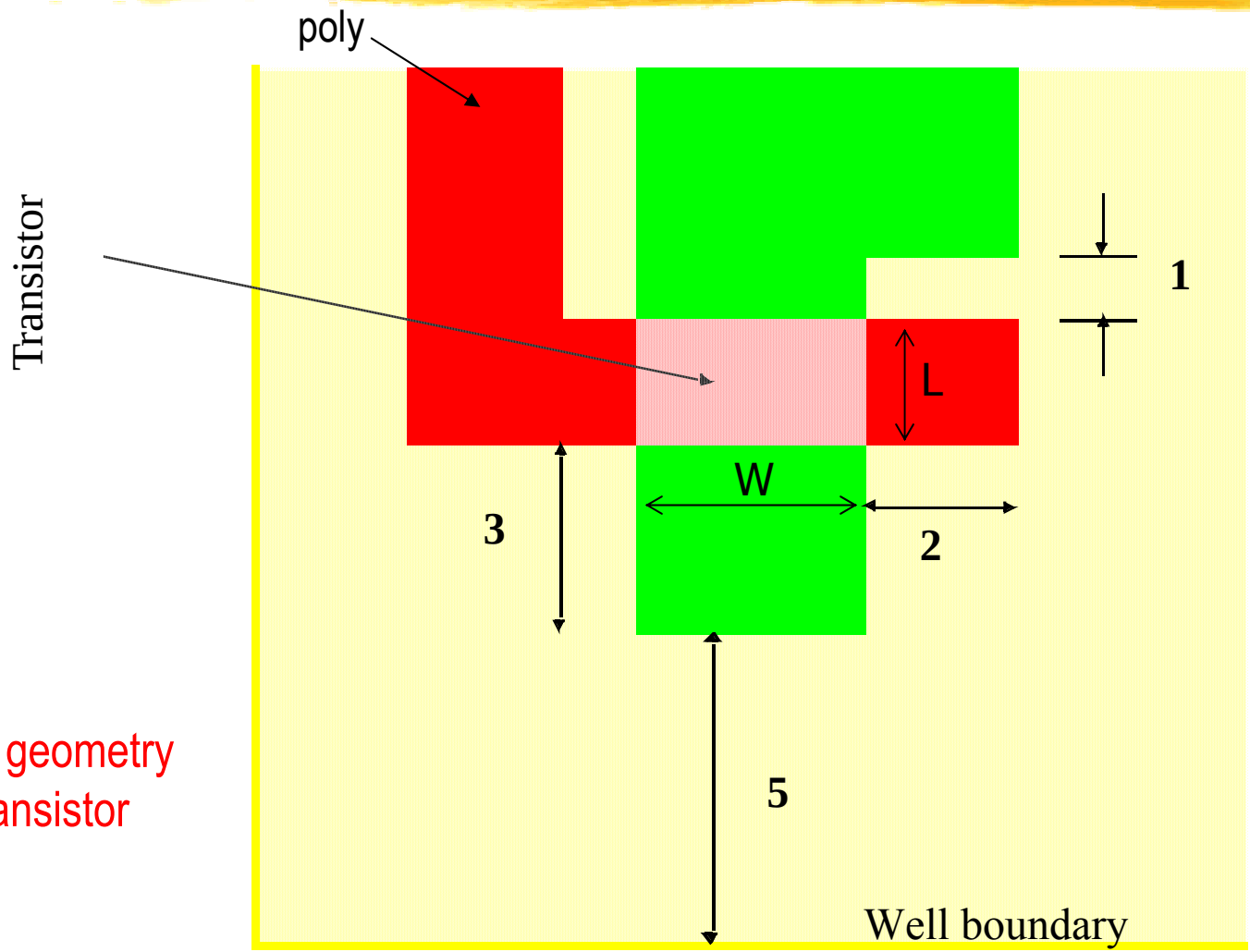
- Interface between designer and process engineer
  - Clean separation between the *process* during wafer fabrication and the *design* effort
    - Permissible geometries -> DESIGN RULES
      - Width rule, space rule, overlap rule, etc.

- Ways to do design rules
  - “Scalable Design Rules”
  - Absolute measures

Scalable Design Rules

- CMOS scales
  - Implement something now, shrink it later
  - Express all design rules in terms of a unit dimension
  - Change the actual dimension of the unit, and the whole design shrinks
  - Mead and Conway
- Unit dimension: Minimum line width (2λ)
  - In 1978, $\lambda = 1.5$ μm (a.k.a. 3 micron technology)
  - In 2003, $\lambda = 0.065$ μm (a.k.a. 0.13 micron technology)
- Important Intellectual idea, not used in industry (but we will)

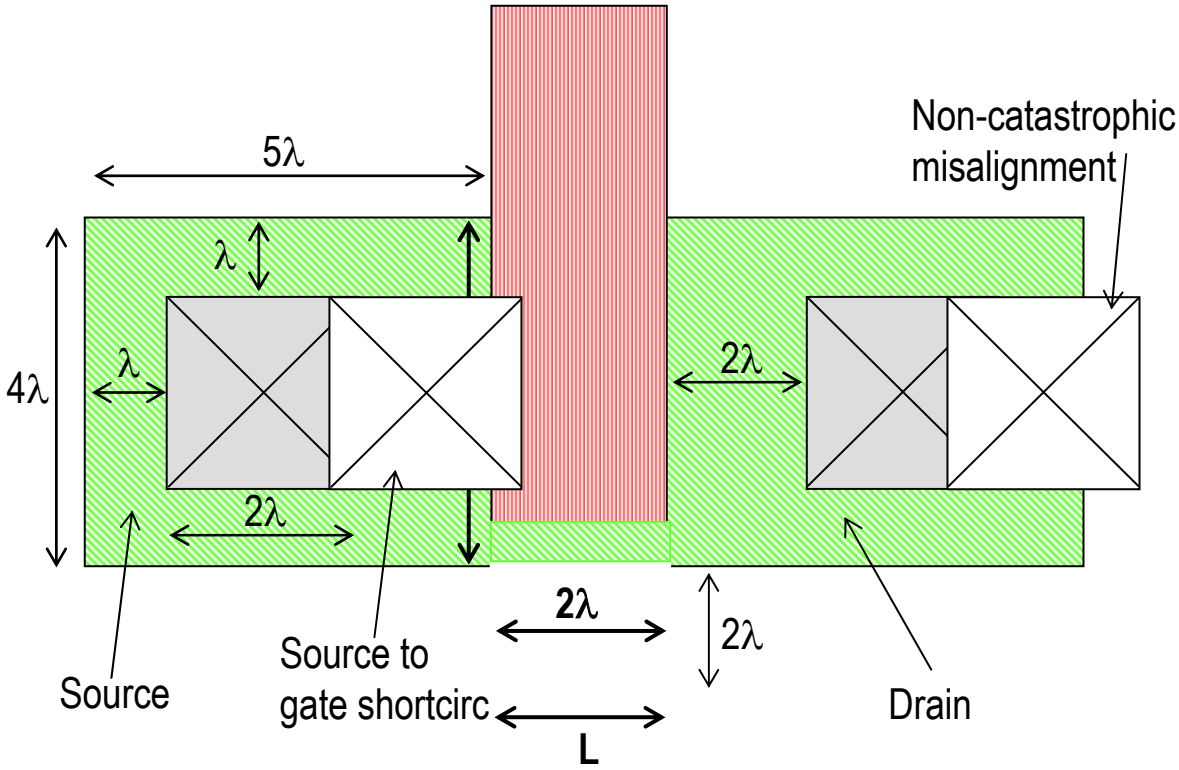
Transistor Layout



The choice of geometry determines transistor parameters!

All distances are expressed in λ

Transistor Layout



$A_S = A_D = 5\lambda W$

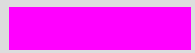
$\lambda = 0.5\mu m \rightarrow A = 12.5\mu m^2$

Absolute Design Rules

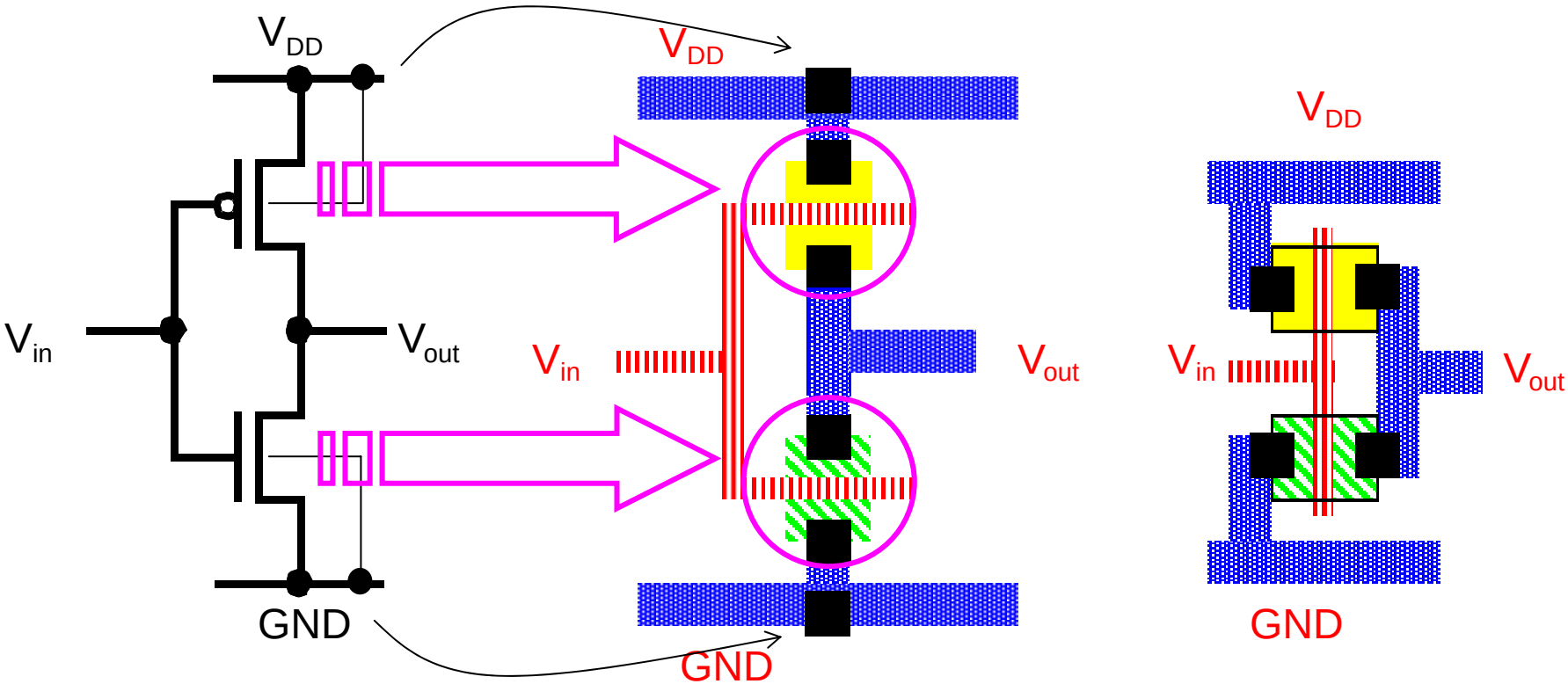
- It is hard to scale every aspect of design linearly
- The elegance of scalable CMOS isn't worth the cost
- Specify all dimensions in real units (μm or nm)

- Currently (0.13 micron), there are THOUSANDS of design rules

CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Inverters

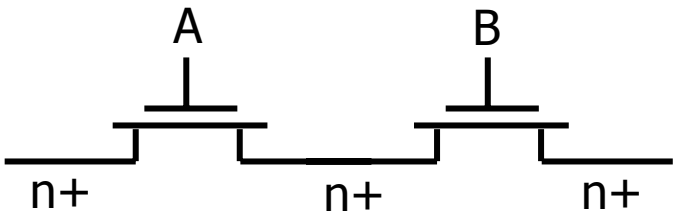


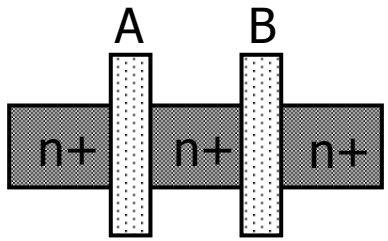
Layout of a NOT gate

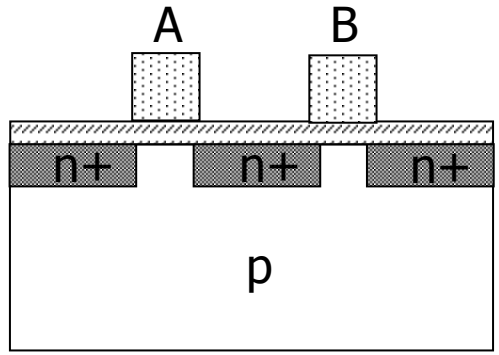
Alternate layout of a NOT gate

Transistor sizing determines inverter fundamental properties!

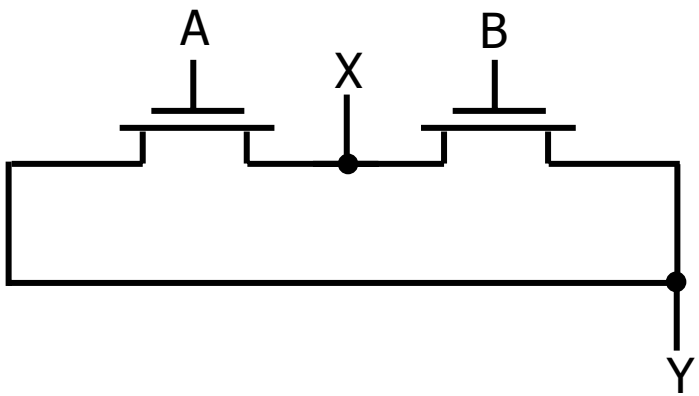
Series/Parallel Connections

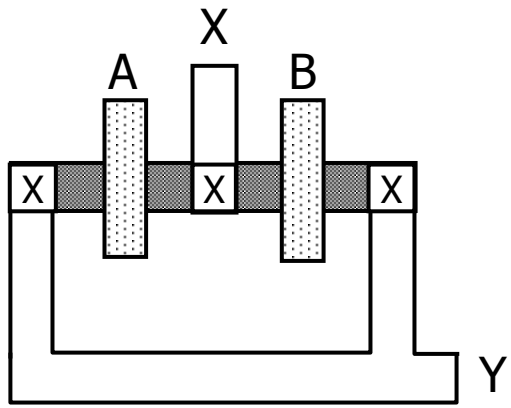






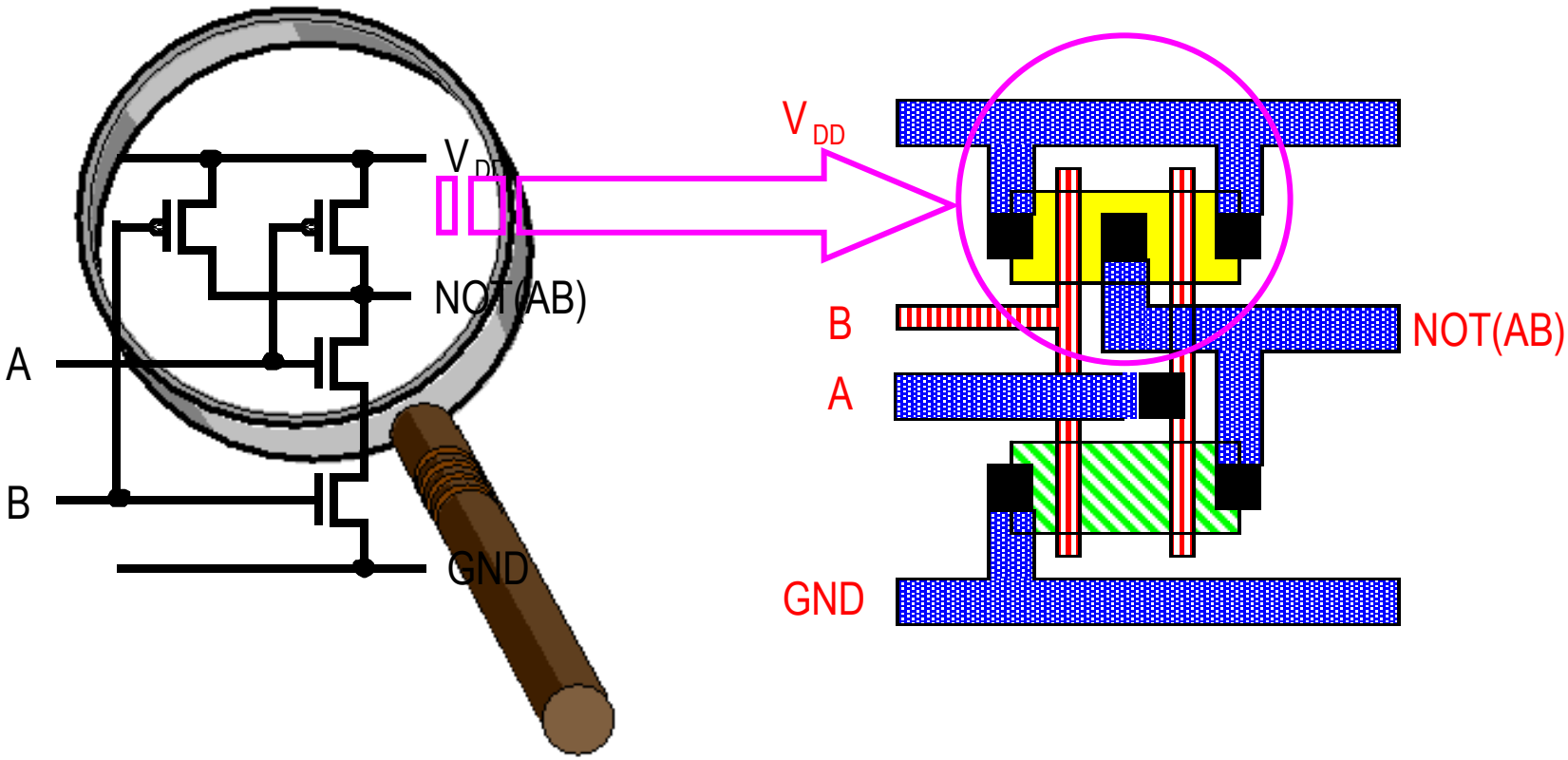
Devices can share patterned regions; this may reduce the layout area or complexity!



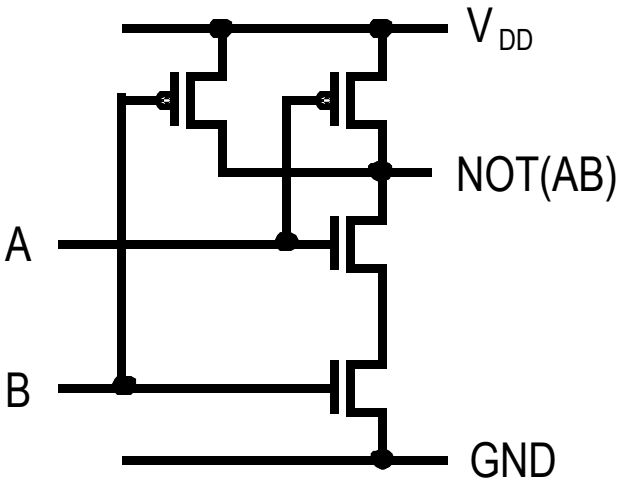


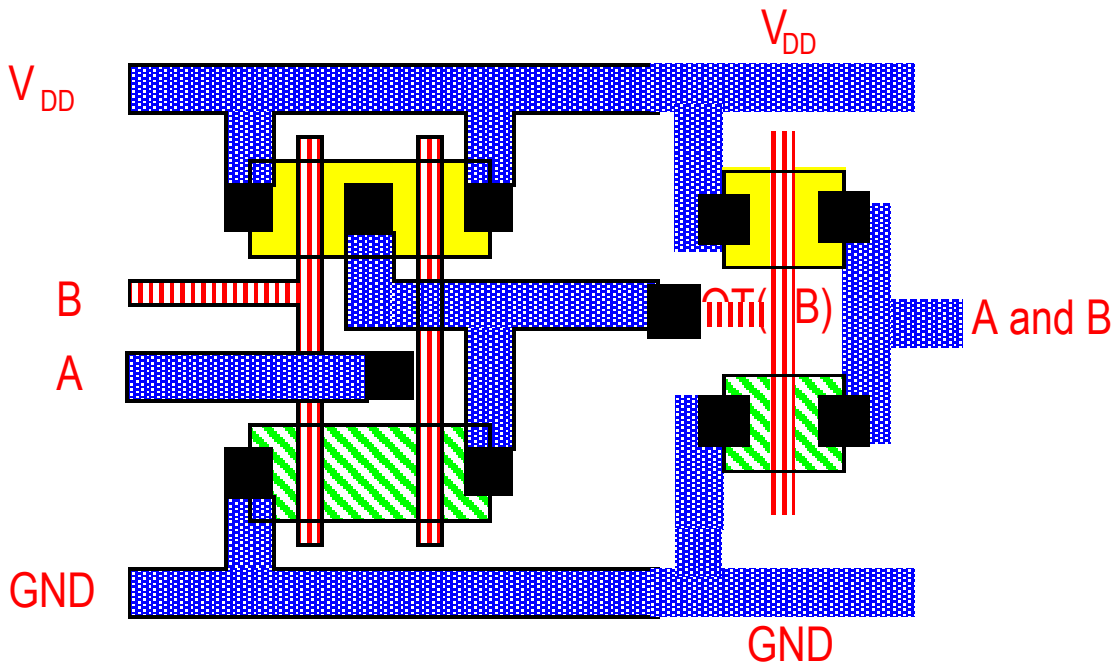
	poly	Red
	n+/p+	Green
	metal	Blue
X	contact	Black

NAND2

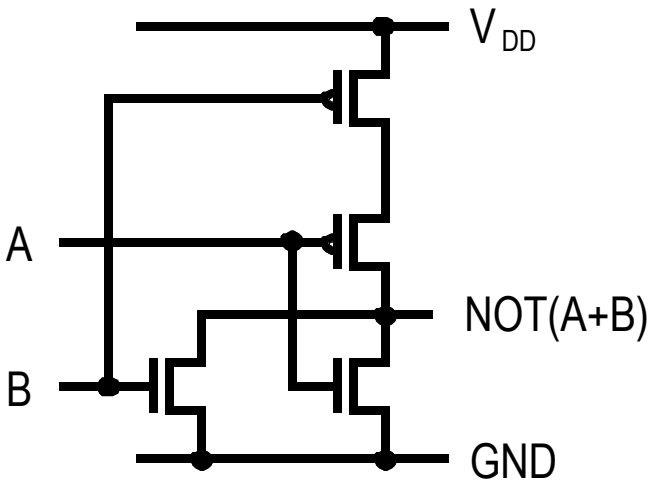


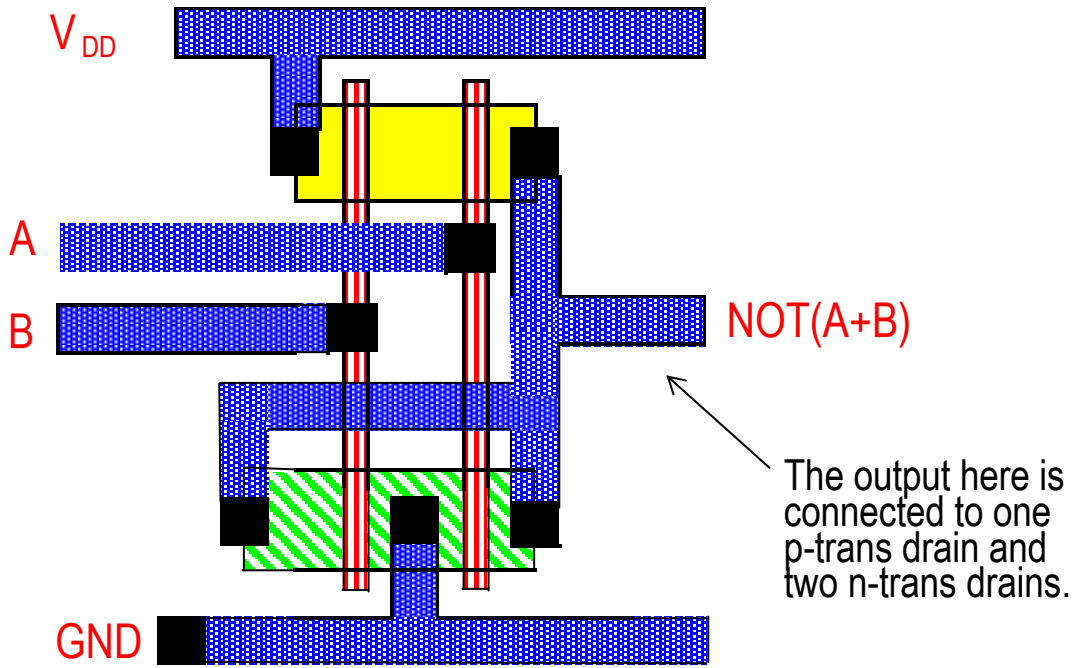
Question: How About AND2?



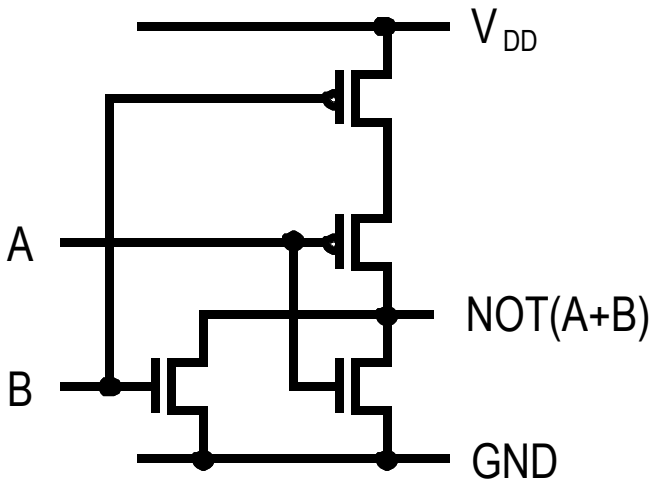


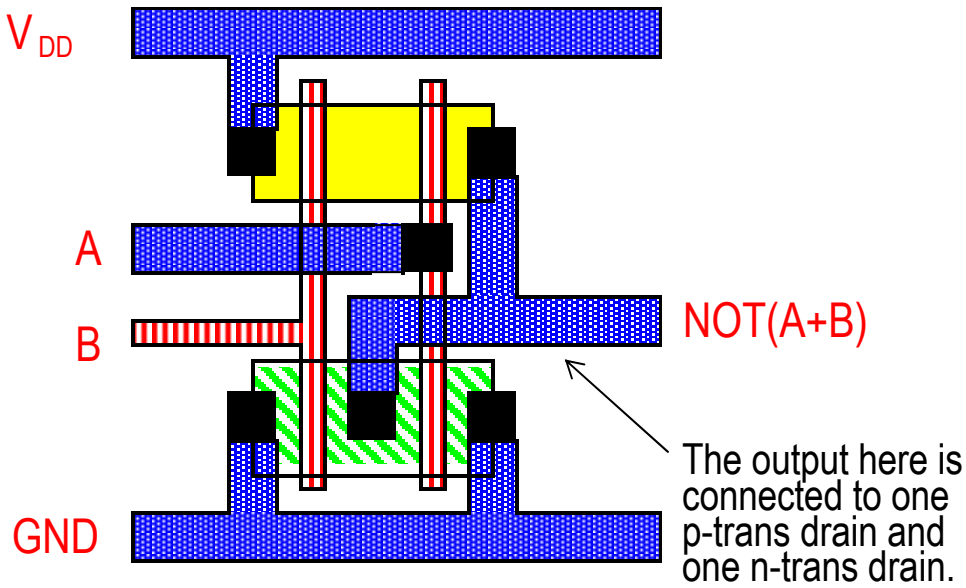
NOR2


V DD
A
B
NOT(A+B)
GND


V DD
A
B
NOT(A+B)
GND
The output here is connected to one p-trans drain and two n-trans drains.

NOR2 (alternate layout)

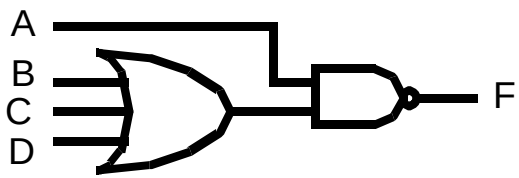




This is better!

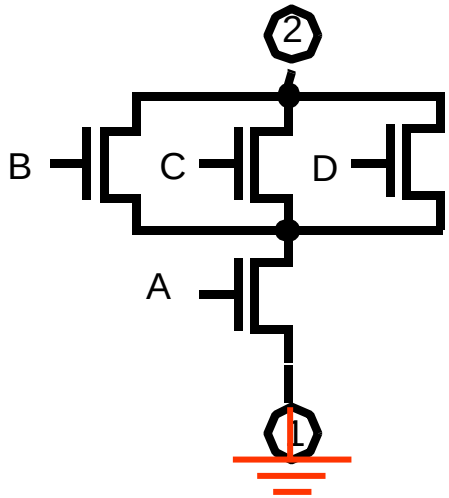
Less drain area connected to the output .
This results in a faster gate.

Complex Logic Gates: OAI Gates

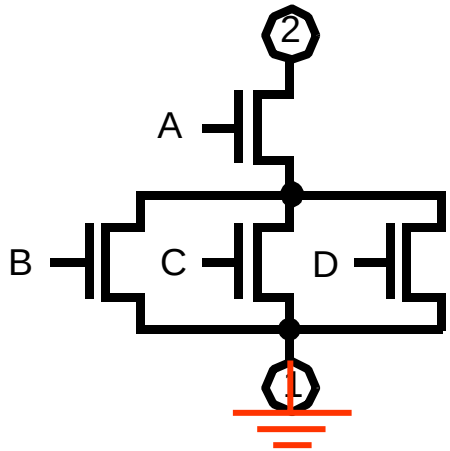


F= NOT(A(B+C+D))

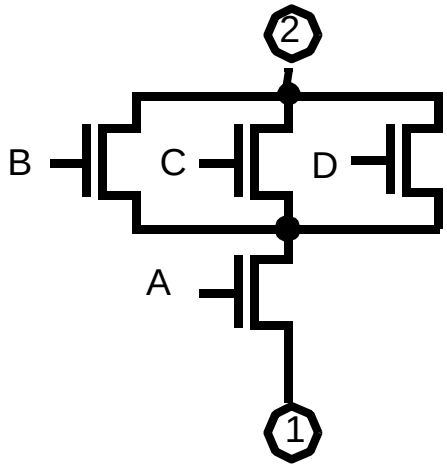
#1

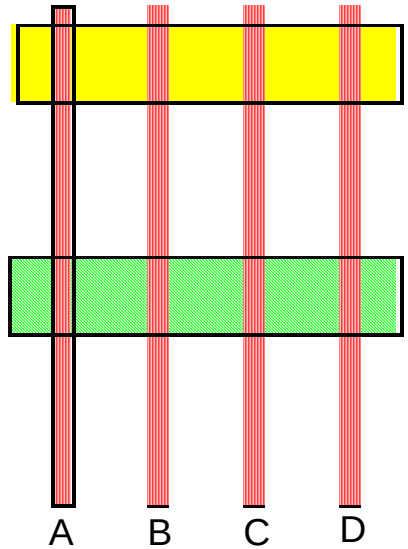


#2

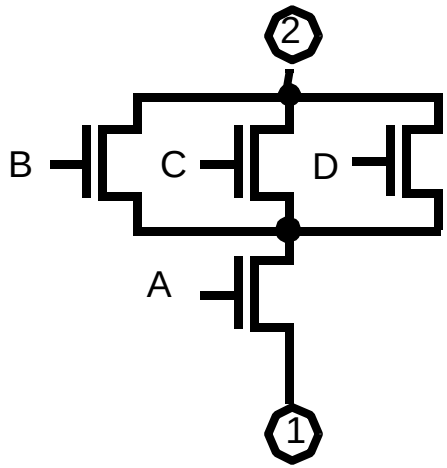


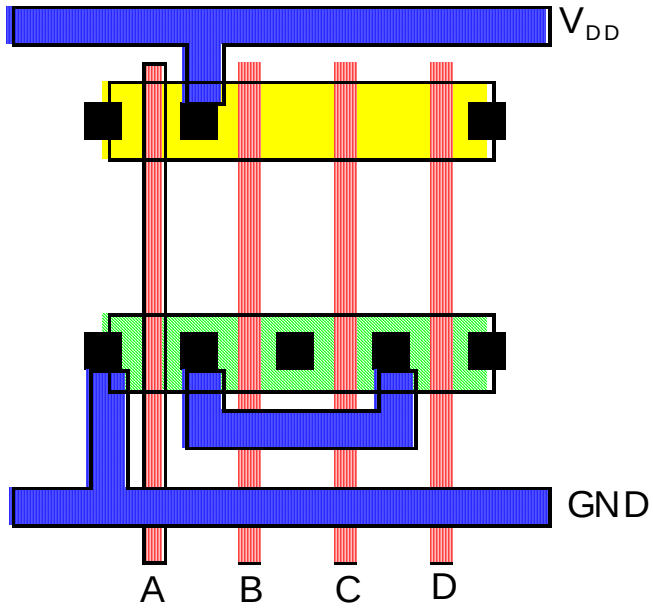
OAI Gates: Sharing S/D (option 1)



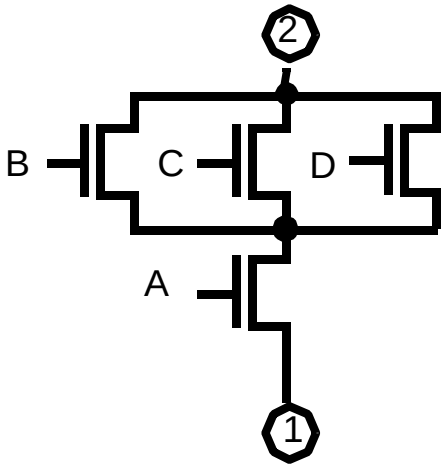


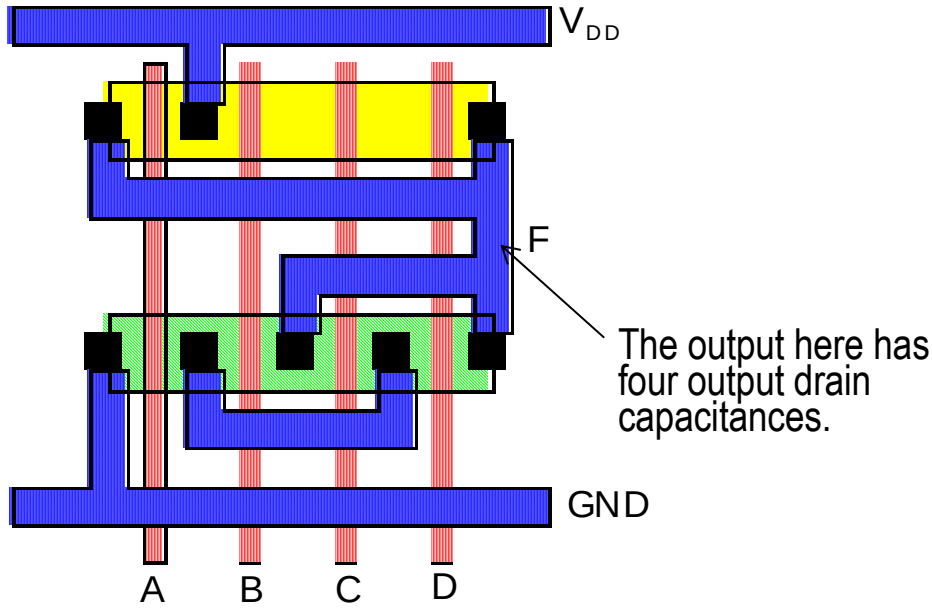
OAI Gates: Sharing S/D





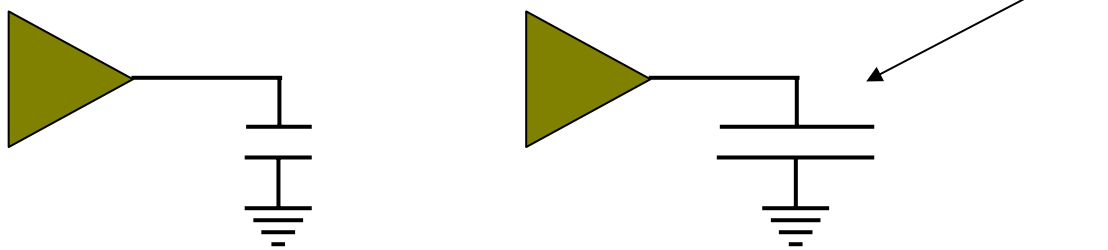
OAI Gates: Sharing S/D





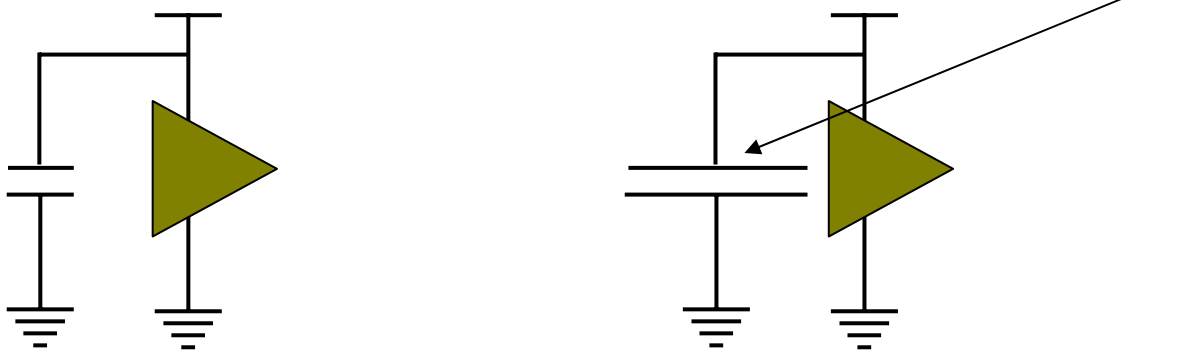
Capacitance: Friend or Foe???

- Foe: Slows down the output:



Big Capacitance
More charge to
to change voltage
SLOWER!

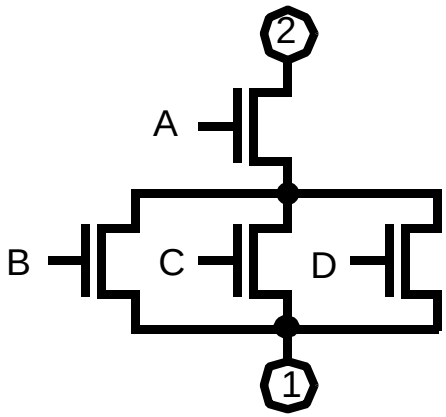
- Friend: Stabilizes the Power Supply

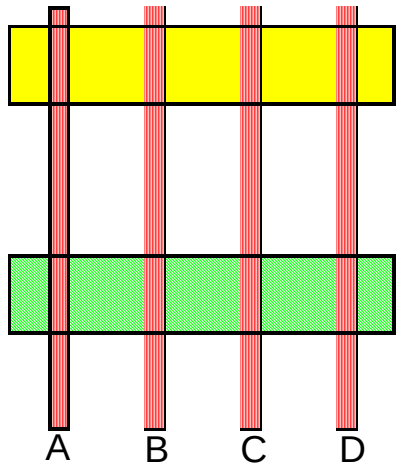


Big Capacitance
More charge to
to change voltage
More stable supply
voltage!

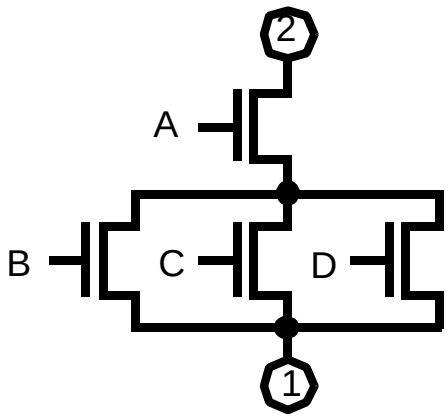
OAI Gates: Sharing S/D (option 2)

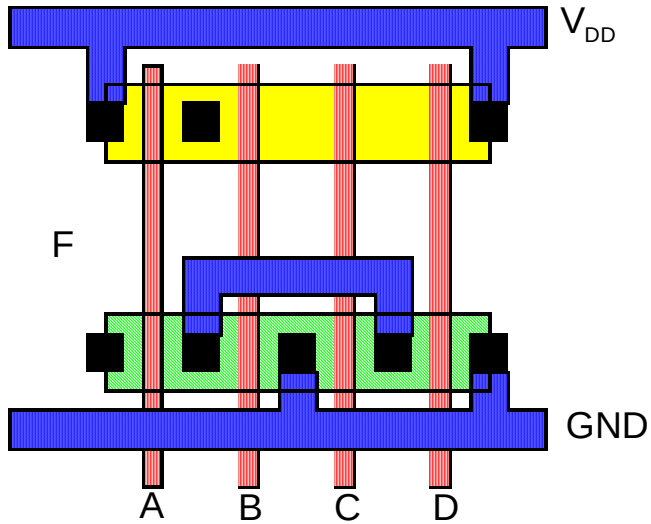
#2



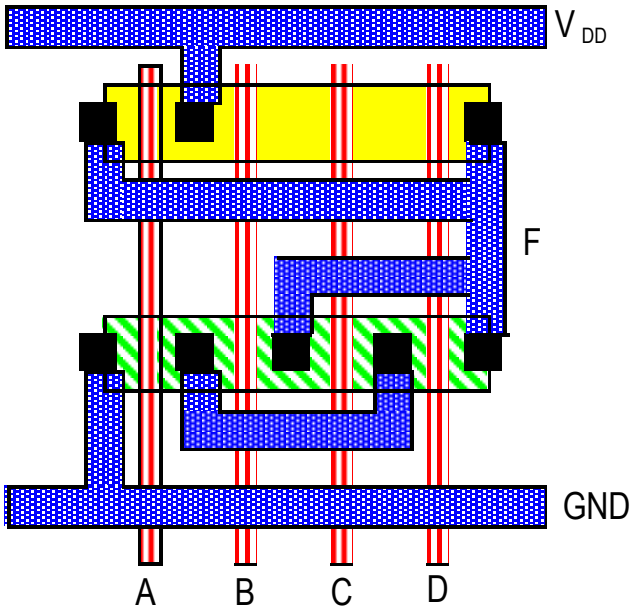


OAI Gates: Sharing S/D



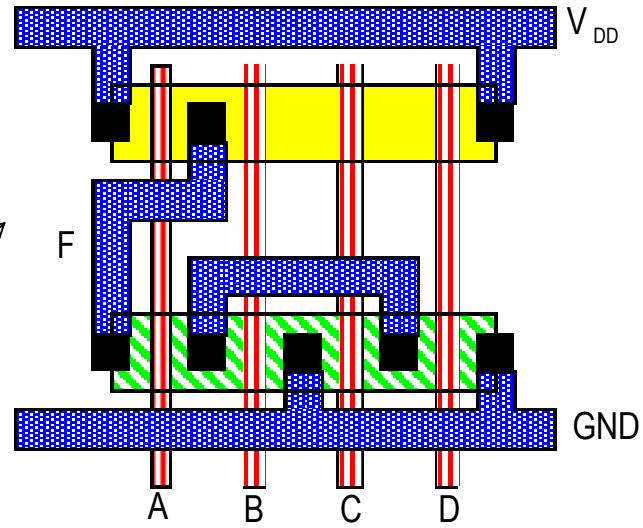


OAI Gates: Sharing S/D



Wrong

The output here has two output drain capacitances.

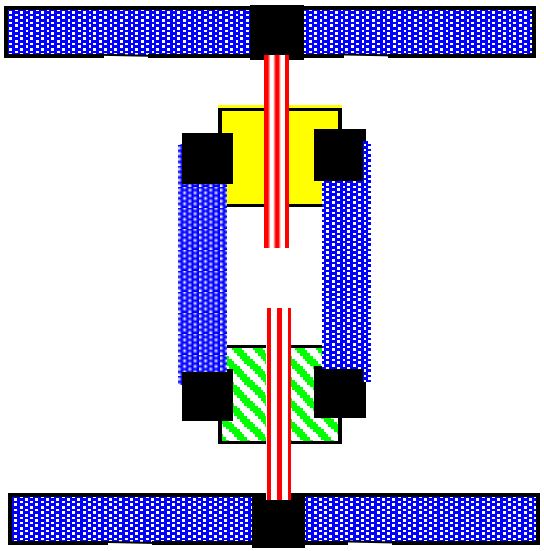


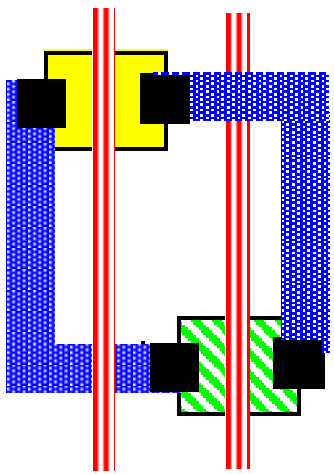
Right

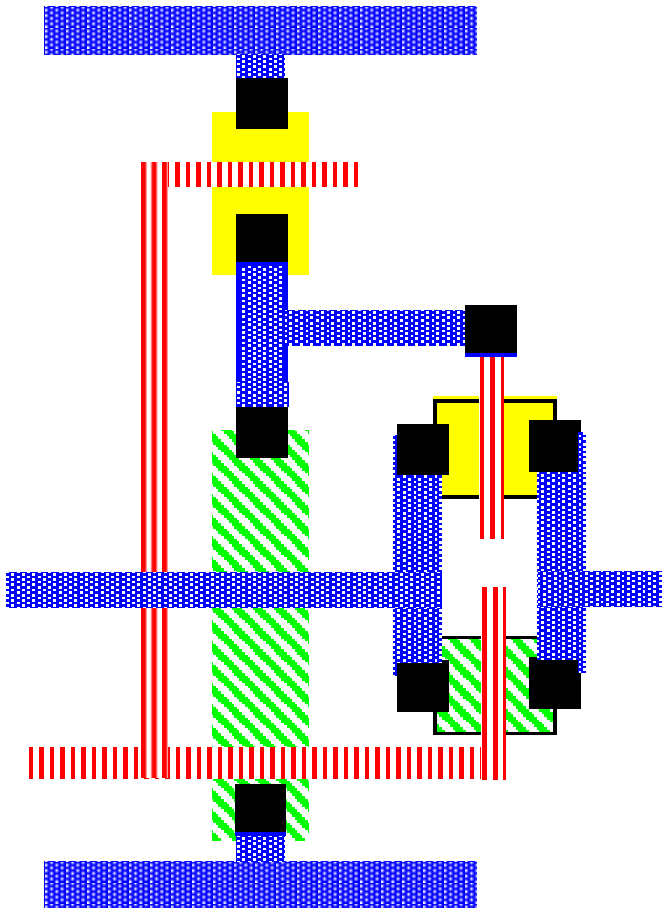
Gate Design Procedure

- Run VDD and GND in metal at top and bottom
- Run vertical poly for each gate input
- Order gates to allow maximum source-drain abutting
- Place max number of n-diffusions close to GND
- Place max number of p-diffusions close to VDD
- Make remaining connections with metal
  - Minimize metal usage

Question: How About TGs?





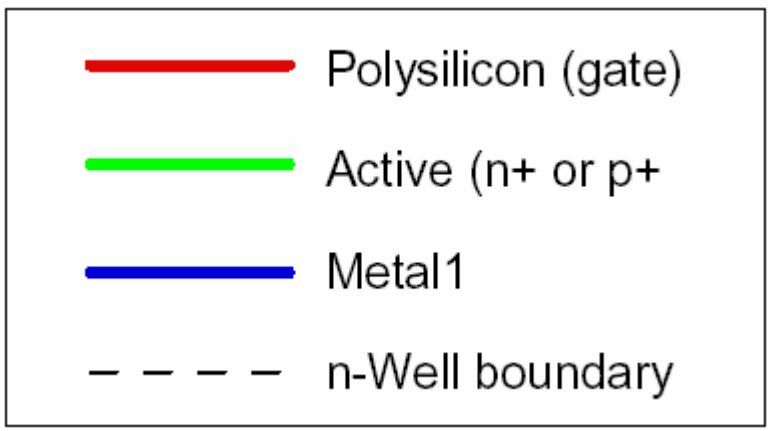


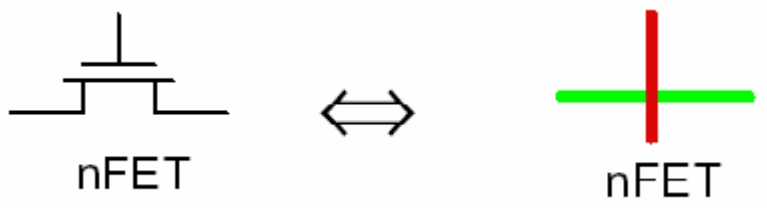
Overview

- ✓ Physical structure of ICs
  - Design rules
  - Basic gates layout
- Stick diagrams
  - Basic rules
  - Examples
- Cadence (Virtuoso)

Stick Diagrams

- Introduced by Mead & Conway in the '80s
- Every line of a conduction material layer is represented by a line of a distinct color





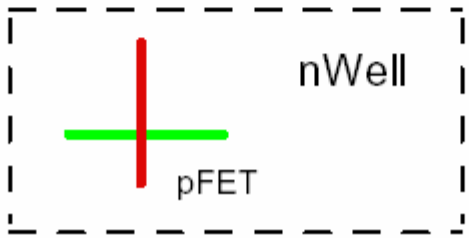
nFET and pFET Representations

In terms of stick diagrams, we thus say that an nFET is formed whenever

Red (Poly) crosses over Green (Active)

This is consistent with a top view of the transistor.

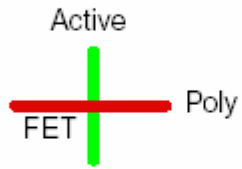
A pFET is described by the same "red over green" coding, but the crossing point is contained within an nWell boundary



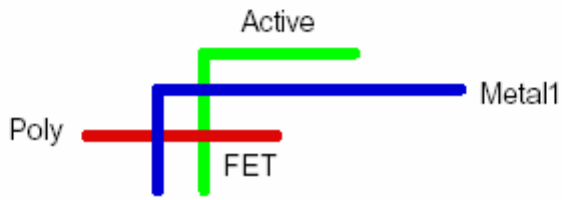
Basic Rules (1)

The rules for constructing stick diagrams are based on the characteristics of the conducting layers.

- Only the routing is important, not the line widths
- Red over green gives a FET
  (Poly) (Active)

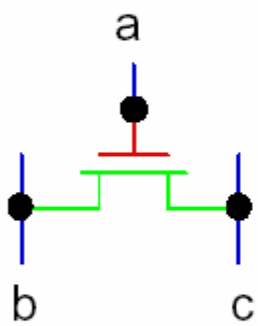


- Blue may cross over green or red without a connection
  (Metal1) (Active) (Poly)

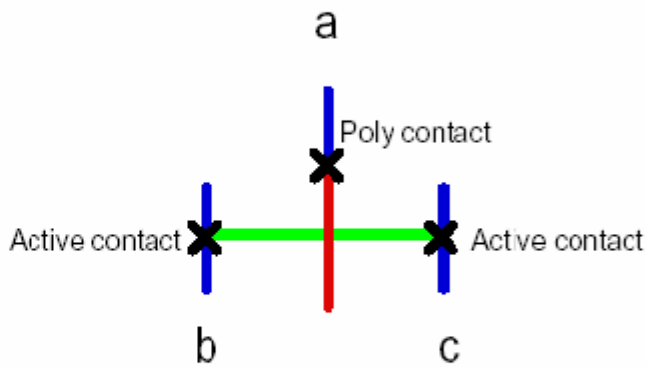


Basic Rules (2)

Connections between layers are specified by ✖



Schematic

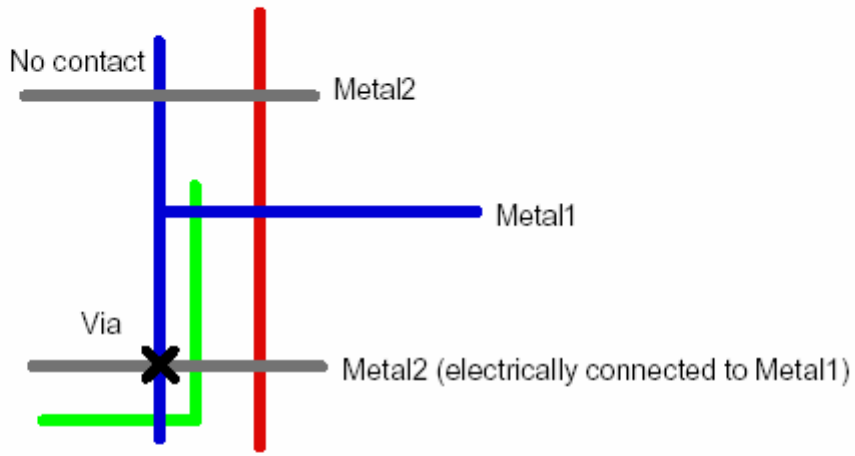


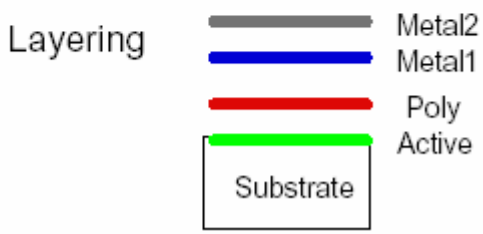
Stick diagram

Poly contact: Metal1-to-Poly
Active Contact: Metal1-to-Active

Basic Rules (3)

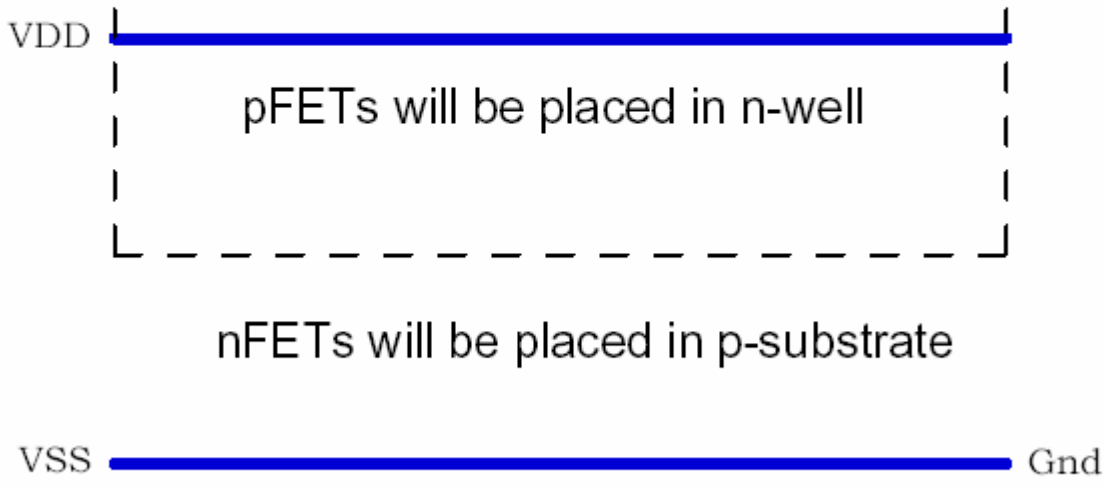
Metal lines on different layers can cross one another.
Contacting two metal lines requires a via





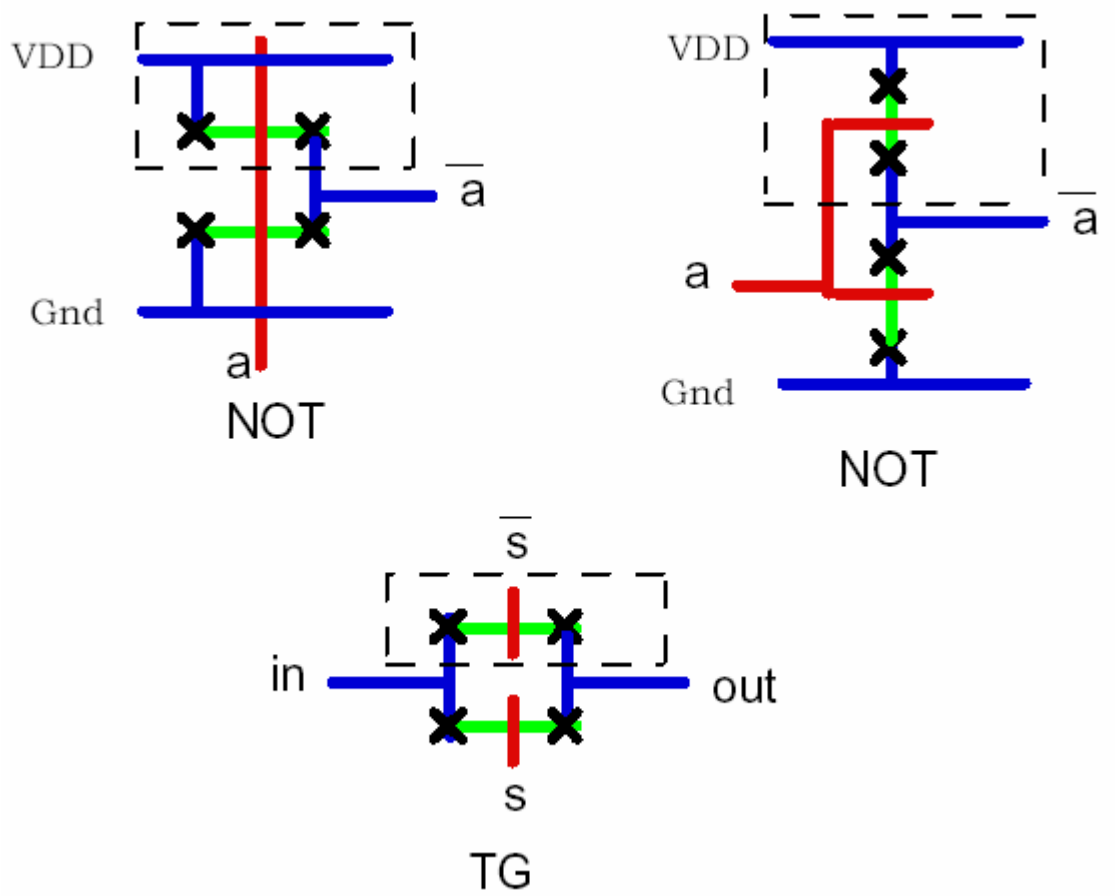
Logic Gates Design

To create CMOS logic gates, we start with the VDD and VSS (ground) lines. We will use a horizontal orientation for the lines. Remember that stick diagrams only deal with the routing. Widths and spacings are not important.



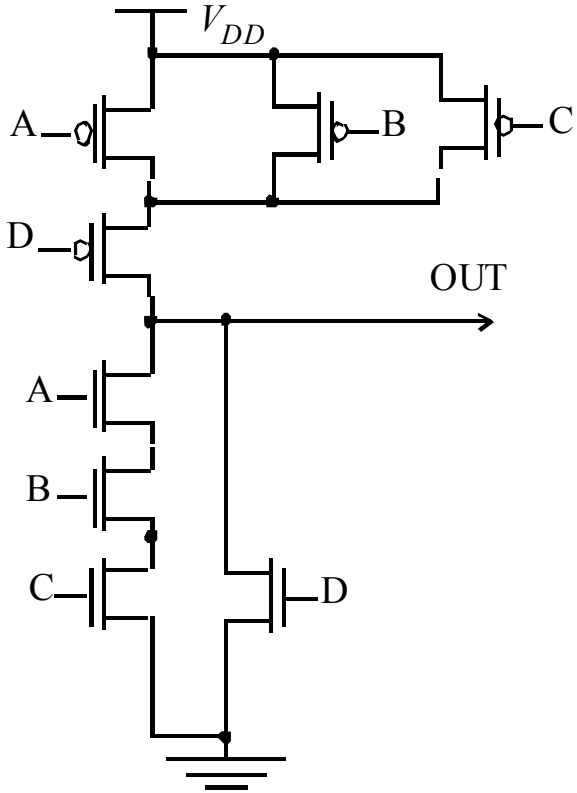
We have included an n-well region around VDD

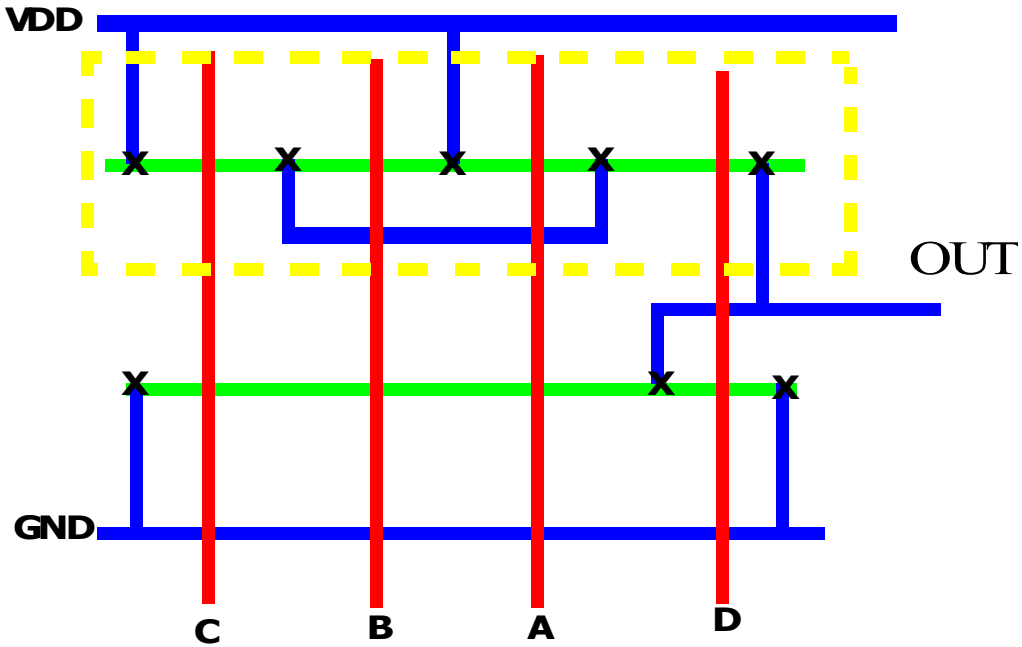
Examples


VDD
$\overline{a}$
Gnd
a
NOT
VDD
$\overline{a}$
a
Gnd
NOT
$\overline{s}$
in
out
s
TG

Complex Functions

$OUT = \overline{ABC + D}$

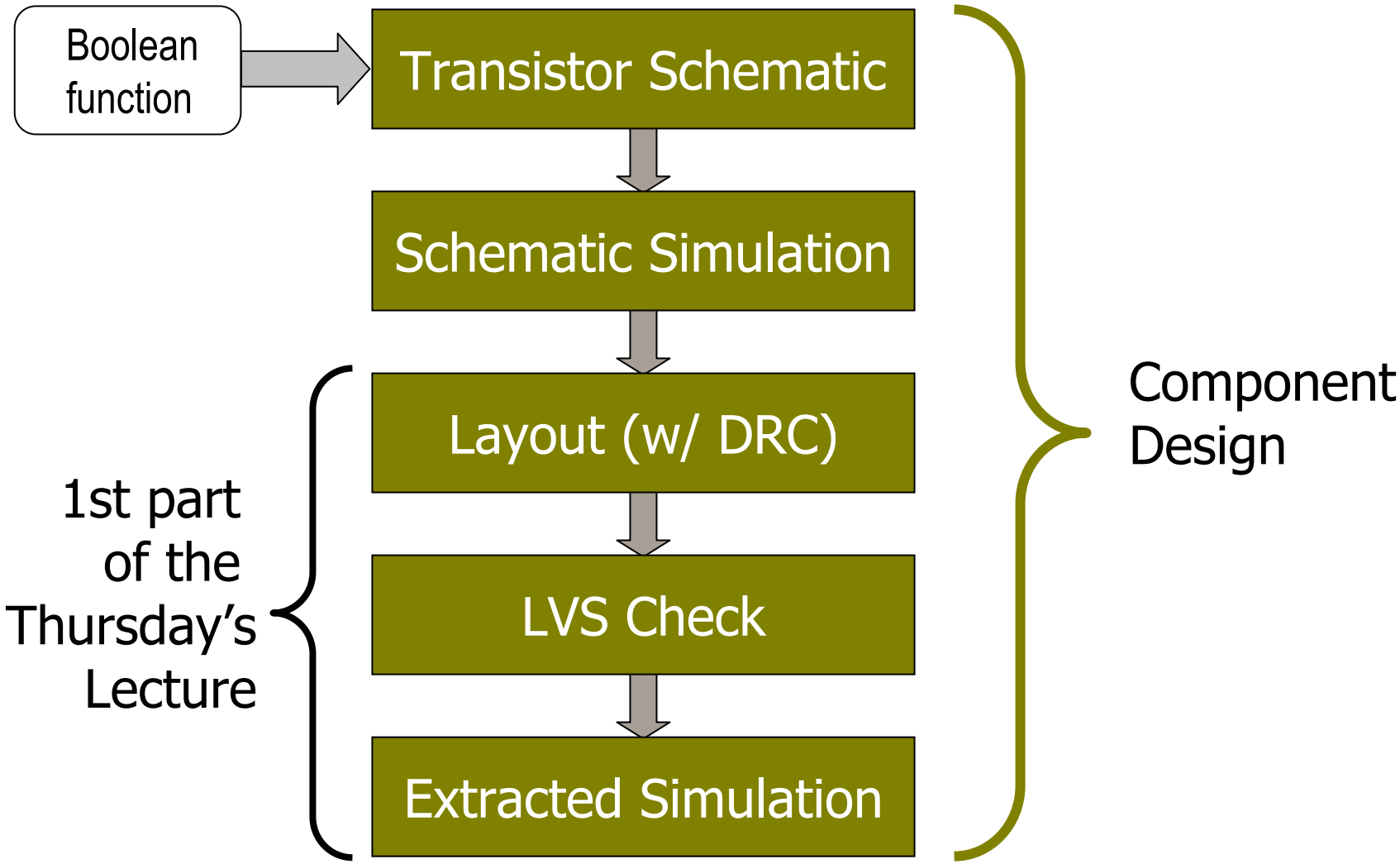




Summary

- Discussed
  - Design rules
  - Basic gates layout
  - Stick diagrams
- Need more practice on
  - Stick diagrams
  - Layout (mostly in the lab)

Preview: The 18-322 Flow



Preview: Modern ASIC Design

- Designer Productivity is a big problem
- In 1978, people could draw transistors, now there are 100s of millions per chip…
- New abstractions necessary: