Memory III: Dynamic Random Access

- Memory Classification
- DRAM basics
  - Single transistor memory cell
  - Memory architecture
- DRAM circuitry
  - Read/refresh operation
  - Charge sharing
  - DRAM design trends/limitations
Memory Classification

- Memories
  - Semiconductor Memories
    - Random Access Memories
      - RAM
    - Other Memories
  - Other Memories
  - Dynamic (DRAM)
  - Static (SRAM)
    - Read Only (ROM)
    - Programmable (PROM)
  - Electrically
  - Erasable EPROM
  - Flash Memories
DRAM basics
Single transistor memory cell

SENSAMP

Leakage!
DRAM basics
Single transistor memory cell
DRAM basics
Single transistor memory cell

Leakage
DRAM basics
Memory architecture

ROW

Word
DRAM circuitry
Read/refresh operation

PRE
SENSAMP
ROWSELECT
VDD
VDD
V
V
L
R
VV LR

BC
D
D
D
D
C/2
CB
C/2
DWL(L) PRE WL(L) D PRE D DWL(L) PRE WL(L) D PRE D
DWL(R) PRE WL(R) D PRE D DWL(R) PRE WL(R) D PRE D

PRE
VDD
DWL(L) WL(R) V L VR SENSAMP ROWSELECT

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DRAM circuitry
Read/refresh operation
DRAM circuitry
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DRAM circuitry
Read/refresh operation

**Diagram:**

- **DWL(L)**
- **PRE**
- **C/2**
- **C_B**
- **WL(L)**
- **D**
- **PRE**
- **SSENSAMP**
- **ROWSELECT**
- **V_L**
- **V_R**
- **VDD**
DRAM circuitry
Read/refresh operation
DRAM circuitry
Charge sharing

Diagram of DRAM circuitry showing DWL(L), PRE, D, WL(R), row select, V_L, V_R, SENSAMP, and C/2.
DRAM circuitry
Charge sharing

\[ V_x = \frac{V_1 \cdot C_1 + V_2 \cdot C_2}{C_1 + C_2} \]
\[ V_x = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2} \]
DRAM circuitry
Charge sharing

\[ V_x = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2} \]

\[ V_{Lx} = \frac{V_{DD} C_B}{C_B + C/2} \quad V_{Rx} = \frac{V_{DD} C_B}{C_B + C} \]

\[ V_{Rx} = \frac{V_{DD} C_B + V_{DD} C}{C_B + C} \]
DRAM circuitry
Charge sharing

\[ V_{Lx} = \frac{V_{DD} \cdot C_B}{C_B + C/2} \quad > \quad V_{Rx} = \frac{V_{DD} \cdot C_B}{C_B + C} \]

\[ V_{Lx} = \frac{V_{DD} \cdot C_B}{C_B + C/2} \quad < \quad V_{Rx} = V_{DD} \]
DRAM circuitry
DRAM design trends/limitations

\[ V_{Lx} = \frac{V_{DD} C_B}{C_B + C/2} > V_{Rx} = \frac{V_{DD} C_B}{C_B + C} \]

Bit line to cell capacitance high ratio !!!
DRAM layout

Active ⇔ Gate oxide ⇔ Poly I
DRAM layout

Poly I ⇔ Oxide ⇔ Poly II
DRAM layout
DRAM layout
DRAM layout
DRAM layout
DRAM layout