Memory I: Overview of Semiconductor Memories

- Random Access Memories
- ROMs:
  - ROM
  - Decoders
  - PLA’s
  - EEPROM
Static Random Access

- Memory Classification
- CMOS Static Memory
  - Six transistor memory cell
  - Memory architecture
  - Decoders
  - Read/write circuitry
- RMOS Static Memory
  - Four transistor memory cell
  - Technology
  - Memory cell layout
Memory Classification

Memories

Other Memories

Semiconductor Memories

Other Memories

Random Access Memories RAM

Dynamic (DRAM)

Static (SRAM)

R/W Memories

Read Only (ROM)

Programmable (PROM)

Flash Memories

Electrically Erasable EPROM (EEPROM)
Memory Classification

Semiconductor Memories

Read Only (ROM)  L 23

Static (SRAM)  L 23/24

Dynamic (DRAM)  L 24
Random Access Memories

 ROW DECODER

 COLUMN DECODER
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)
Row Decoder

A₀ A₁ R₀ R₁ R₂ R₃
Column Decoder
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)

Metal
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)
Read Only Memory (ROM)
Programmable Logic Array (PLA)
Programmable Logic Array (PLA)
PLA

\[ A + B = A \bar{B} \]

\[ \bar{A} + B = \bar{A} B \]
OR

VDD

VDD

X

Y

X+Y

PLA
PLA

A + B = A\ B
A + B = \overline{A} \overline{B}

VDD

\overline{A} + \overline{B} = AB
A + B = \overline{A} \overline{B}

AB + \overline{A} \overline{B} \quad \overline{A} + B
PLA
Metal

PLA
PLA
PLA
PLA
Electrically Programmable

Control Gate

Floating Gate

Source       Drain

"n"             "p"             "n"

Erase  --> Apply UV
         --> Low Vt --> Transistor ON when Selected

Program --> CG = High, Drain = High, Source = Low
         --> High Vt --> Transistor OFF when Selected
Electrically Programmable

Erase --> CG = High, Drain = Low, Source = Low
--> High Vt --> Transistor OFF when Selected

Program --> CG = Low, Drain = High, Source = Low
--> Low Vt --> Transistor ON when Selected
Electrically Programmable
Flash EEPROM

- Same as EEPROMs
- Erased in Single Cycle
- Relatively low number of erase/program cycles
Static Random Access Memories

- Memory Classification
- CMOS static memory
  - Six transistor memory cell
  - Memory architecture
  - Decoders
  - Read/Write circuitry
Memory Classification

- Memories
  - Semiconductor Memories
    - Random Access Memories
      - Dynamic (DRAM)
        - Static (SRAM)
          - R/W Memories
            - Read Only (ROM)
              - Programmable (PROM)
                - Electrically Erasable EPROM
  - Other Memories
    - Flash Memories
CMOS static memory
Six transistor memory cell
CMOS static memory
Six transistor memory cell
CMOS static memory
Memory architecture

![CMOS static memory diagram](image)
CMOS static memory
Decoders
CMOS static memory
Read/Write circuitry

Data in

W/R

From column
decoder

Diff. Amplifier

Bit

Bit

OUT

GND
CMOS static memory

Read

Data in

W/R

From column decoder

Diff. Amplifier

OUT

GND
CMOS static memory

Write

Data in

W/R

From column decoder

GND

Bit

Bit

Diff. Amplifier

OUT