Beyond The Basic Gates
Outline

• How to make larger blocks?
  – Rotating/mirroring cells
  – Abutment & Power/ground rails
  – Substrate contacts
• Floorplanning
  – Routing channels
  – Block porosity
  – Metal layer allocation
• Buffering
  – Large Loads
  – Long Lines
  – Folding Transistors
Rotating / Mirroring Cells

- Why we rotate/mirror cells
  - Allows us to make cells in one orientation and use them in a different one
  - Allows us to line up vdd and gnd rails so we can overlap them. (useful for abutment)
  - In general, it allows you to be creative in your designs without making you create a new cell for each orientation
Abutment

• What is abutment?
  – Designing the outputs of a module to line up with the inputs of the next module

• Why should I use abutment?
  – It makes designs more dense
  – It makes creation of large components easy
  – Some of Signal/Power routing can be done automatically
Partial Layout – Register

This is just a sample cell

Clock
Reset

Vdd!
Gnd!
Abutted – Registers

Note: every other cell is mirrored along the y-axis to facilitate this abutment.
Abutted – Registers (cont)
Vdd and Gnd Rails

Vdd!  Gnd!
Vdd and Gnd Rails
Substrate Contacts
Layout Design Flow

Use floorplan to determine component sizes

Floorplan

Use component sizes to revise and optimize floorplan

Layout
Layout Design Flow

- Use floorplan to determine component shapes.
- Simulate to determine optimal transistor sizing.
- Revise sizings and resimulate until optimal.
- Use final component sizes to revise and optimize floorplan.
Porosity/Routing Channels

- Ability to get wires through a block
- A zero-porosity example:

How to get wire from here

To here?

If the cells don’t use a metal layer then route directly. Maybe design the cells such that they don’t use a metal layer?
Floorplanning with Routing Channels

PLAN!
- Estimate sizes of wires/busses
- Allocate space on layers
- Attempt to localize connections
- Attempt to run wires on top of logic instead of channels (i.e. porosity)

Routing Channel
You are free to use this space however you feel fit.
Needed abutment in your design

Abutment
Driving Large Capacitances

PROBLEM

Input waveform

Output waveform

minimum sized inverter can not drive large loads efficiently
Optimal Number of Stages

\[ u_{opt} = e \text{ (can just use 3)} \]

\[ N = \ln\left(\frac{C_L}{C_i}\right) \]

\[ t_p = e \cdot \ln\left(\frac{C_L}{C_i}\right) \cdot t_{p0} \]
Driving Distributed Loads
Driving Long Wires

\[ \text{Delay} = \frac{rc}{2} L^2 \]

\[ \text{Delay} = t_{\text{inv}} + 2 \times \frac{rc}{2} \left(\frac{L}{2}\right)^2 \]
Designing Large Buffers
Folding Transistors

min-size inverter
max-sized inverter
2*max-sized inverter
4*max-sized inverter