Problem 1. (30 points) A two-stage buffer is used to drive a metal wire of 1 cm. The first inverter is of minimum size with an input capacitance $C_i=10$ fF and an internal propagation delay $t_{p0}=50$ ps and load dependent delay of $5$ ps/fF. The width of the metal wire is $3.6$ µm. The sheet resistance of the metal is $0.08\, \Omega/\square$, the capacitance value is $0.03\, fF/\mu m^2$ and the fringing field capacitance is $0.04 fF/\mu m$.

a) What is the propagation delay of the metal wire?

b) Compute the optimal size of the second inverter. What is the minimum delay through the buffer?

Problem 2. (30 points) Convert the following RTL module to a gate level design.

```vhdl
module xx(a, b, c, d, e, f);
    input a, b, c;
    output d, e, f;
    reg e, f;
    assign d = ~(b & c);
    always @(posedge clk)
    begin
        if (a === 1) then
            begin
                e <= b ^ c;
                f <= c;
            end
        else
            begin
                e <= f & c;
                f <= d;          // Line X
            end
    end
endmodule
```

a) Show your results with a schematic. Label all wires or input/output ports with the names given in the RTL code.

b) (Difficult) If Line X is removed from the RTL, what does this imply about how the gate-level design should work? Draw a modified schematic.

Problem 3. (20 points) A component in a microprocessor performs a combinational function on every instruction. Assume this combinational function takes 20 ns to compute. We want to pipeline this computation in order to increase the clock cycle. The setup time to the DFFs in our library is 1ns, the clock-to-q delay is 2ns.
a) Graph the latency of the computation (the time it takes to perform one function on one block of data) with pipeline stages from 1 (no pipelining) to 10. Assume that it is possible to break the computation up perfectly evenly into as many pipeline stages as you want.

b) Graph the throughput (the number of computations performed per second) as a function of the pipeline stages from 1 to 10.

**Problem 4.** (20 points) In figure below, the propagation delay of each gate is shown either above or inside the gate in terms of some time unit. Determine the length of the critical path in time units through the logic from any input to any output. HINT: Make sure that your answer is not a false path. That is, make sure that your critical path can logically occur.