

# CURRICULUM VITAE

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## Education

- Ph.D. in Computer Engineering, University of Southern California - August 1998  
Dissertation: *Information-theoretic and Probabilistic Measures for Power Analysis of Digital Circuits*  
Advisor: Prof. Massoud Pedram
- M.S. in Computer Science (Eng. Dipl.), Polytechnic Institute of Bucharest, Romania - June 1991  
Dissertation: *Fault-tolerant Database System Design*  
Advisor: Prof. Irina Athanasiu

## Research Interests

- *Sustainable and Energy-Aware Computing*
  - Smart-grid aware power management solutions
  - Energy-aware general purpose and embedded applications
  - Advanced power management mechanisms for voltage-frequency island based systems
  - Fast and accurate power estimation tools
- *Reliability- and Variability-Aware System Design*
  - Modeling, analysis, and optimization of soft-error rate in large digital circuits
  - Microarchitecture to system level design variability modeling and mitigation
- *Discrete modeling and analysis of signal transduction (STNs) and gene regulatory networks (GRNs)*
  - Boolean modeling and hardware emulation for efficient STN/GRN analysis

## Appointments

- Carnegie Mellon University, Department of Electrical and Computer Engineering  
(Professor, July 2009-Present; Systems Area Leader, Center for Silicon Systems Implementation, August 2008-present; Associate Professor, July 2005 – July 2009; Assistant Professor, March 2000 – July 2005)
  - Currently conducting research on smart grid-aware power management, variability-/reliability-aware system design, and modeling/analysis of STNs/GRNs.
  - Conducted research on energy-aware computing and power efficient processor design, as well as novel microarchitecture design paradigms for high-performance/low power processors and ambient intelligent systems
- University Joseph Fourier and CEA/LETI, Grenoble, France  
(Visiting Professor, June-July 2010; Hosts: Dr. Ahmed Jerraya and Dr. Fabien Clermidy)
  - Conducted research on dynamic power management for 3D chip multiprocessors.
- Technical University Munich, Dept. of Electrical and Computer Engineering, Munich, Germany  
(Visiting Professor, April-July 2009; Host: Prof. Ulf Schlichtmann)
  - Conducted research on variability- and reliability-aware system design.
- University of Maryland, Department of Electrical Engineering

*(Assistant Professor, August 1998 - February 2000)*

- Conducted research projects on theoretical aspects of power analysis and optimization, energy-aware code optimization for superscalar processors, profile-driven compile-time power management techniques
- University of Southern California, Department of Electrical Engineering-Systems  
*(Research Assistant, Spring 1994 - August 1998)*
  - Participated in the design and implementation of POSE (Power Optimization and Synthesis Environment), developed at University of Southern California
  - Contributed to the design and implementation of the code for constrained sequence generation/compaction and probabilistic analysis of FSMs
- Research Institute for Building Design (C.O.C.C.), Bucharest, Romania, Software Tools Lab.  
*(Software Engineer, September 1991 - January 1992)*
  - *Designed and implemented a software product for standard representations*

## Teaching Experience

- Carnegie Mellon University, Department of Electrical and Computer Engineering  
*(Professor, July 2009-Present, Associate Professor, July 2005 – July 2009; Assistant Professor, March 2000 – July 2005)*
  - *Spring 2011*: Taught “VLSI CAD: Logic to Layout,” graduate-level course
    - Includes teaching, advising and project coordination for up to 35 undergraduate and graduate students;
  - *Spring 2005-2006, Fall 2001-2003, Fall 2009-2011*: Taught “Energy Aware Computing,” graduate-level course
    - Includes teaching, advising and project coordination for up to 35 undergraduate and graduate students;
  - *Fall 2005, Spring 2008, Spring 2010*: Taught “Fundamentals of Computer Engineering,” sophomore-level course
    - Includes teaching, advising and project coordination for up to 90 undergraduate students;
  - *Fall 2007*: Taught “Advanced Computer Architecture,” graduate-level course
    - Includes teaching, advising and project coordination for 23 undergraduate and graduate students;
  - *Fall 2006*: Taught “Advanced Digital Design Project,” capstone design course
    - Includes teaching, advising and project coordination for 28 undergraduate and graduate students;
  - *Fall 2004*: Taught “Verification of Computer Systems,” senior-level course
    - Includes teaching, advising and project coordination for up to 15 undergraduate students
  - *Spring 2001-2003, Fall 2000*: Taught “Intro to Computer Architecture,” junior-level course
    - Includes teaching, advising and project coordination for up to 70 undergraduate students;
- University of Maryland, Department of Electrical Engineering  
*(Assistant Professor, Fall 1998 – February 2000)*
  - *Fall 1999*: Taught “VLSI System Design Laboratory,” senior-level capstone design course
    - Includes teaching, advising and project coordination for 14 undergraduate and graduate students;
  - *Fall 1998*: Taught “Advances in Low-Power Design Methodologies,” special topics graduate-level course
    - Includes teaching, advising and project coordination for 7 graduate students;

- Involved in improving the Computer Engineering curriculum, especially in completely revamping of the “Computer-Aided Design of Digital Systems” course (taught starting Spring 1999).
- New York University, Department of Computer Science  
(*Teaching Assistant, Fall 1993*)
  - Taught “Programming Languages,” graduate-level course
- Polytechnic Institute of Bucharest, Romania, Department of Computer Science  
(*Teaching Assistant, January 1992 - August 1993*)
  - Taught “Formal Languages and Compiler Design,” “Programming Techniques,” “Data Structures and Algorithms,” “System Modeling and Simulation”

## Awards and Honors

- **Best Paper Award, IEEE Trans. on Very Large Scale Integrated Systems** (2011)
- **ACM-SIGDA Distinguished Service Award** (2010)
- **Best Paper Award, IEEE Intl. Symp. on Quality in Electronic Design** (2009)
- Best Paper Award Nomination, *IEEE Design, Automation and Test in Europe Conference* (2009)
- **Best Paper Award, IEEE Intl. Conf. on Computer Design** (2008)
- Two Best Paper Award Nominations, *45<sup>th</sup> ACM/IEEE Design Automation Conference* (2008)
- Best Paper Award Nomination, *44<sup>th</sup> ACM/IEEE Design Automation Conference* (2007)
- Best Paper Award Nomination, *IEEE Intl. Symp. on Quality in Electronic Design* (2007)
- Best Paper Award Nomination, *IEEE Transactions on VLSI Systems* (2006)
- **Best Paper Award, IEEE/ACM Asian-South Pacific Design Automation Conference** (2005)
- Best Paper Award Nomination, *IEEE Design, Automation and Test in Europe Conference* (2005)
- Elected Chair, Special Interest Group on Design Automation, Association for Computing Machinery (ACM-SIGDA) (2005)
- **Carnegie Institute of Technology George Tallman Ladd Research Award** (2004)
- IEEE-Circuits and Systems Society Distinguished Lecturer (2004-2005)
- ACM-SIGDA Technical Leadership Award (2001-2003)
- **NSF Faculty Early Career Development Award** (2000-2004)
- Best Paper Award Nomination at the *34<sup>th</sup> ACM/IEEE Design Automation Conferences* (1997)
- Best Paper Award Nomination at the *33<sup>rd</sup> ACM/IEEE Design Automation Conferences* (1996)
- Special Mention at the “Traian Lalescu” National Student Contest on Mathematical Sciences, Bucharest, Romania (1988)
- **First Prize at the “Traian Lalescu” National Student Contest on Mathematical Sciences, Cluj-Napoca, Romania** (1987)

## Awards and Honors - Advised Students

- Research Advisor for Lockheed-Martin Eta Kappa Nu Second Prize Winners Archa Jain, Neereja Sundaresan, “Parameterizable On-Chip Communication Synthesis for Multi-Core Systems” (2011)
- Liang Ji-Dian Fellowship for Ph.D. Student Kai-Chiang (Alex) Wu (2011)
- Angel G. Jordan Award for Ph.D. Student Siddharth Garg (2010)
- Intel Foundation Ph.D. Fellowship for Ph.D. Student Sebastian Herbert (2007-2009)
- Lamme-Westinghouse Fellowship for Ph.D. Student Phillip Stanley-Marbell (2005-2006)
- Research Advisor for CIT Meeting of the Minds Third Prize Winner Jianjian Sun, “Deployment of Low Power Modes for E-Textile Applications” (2005)
- Research Advisor for CIT Meeting of the Minds First Prize Winners Justin Ang and Shing-Tai Leung, “Energy Aware Computer Arithmetic Modules” (2002)

- Research Advisor for Lockheed-Martin Eta Kappa Nu Third Prize Winner Shing-Tai Leung, “A Library of Energy Aware Computing Gates” (2002)

## **Press Coverage and Discussion of Investigator’s Research**

- “Variability modeling moves to system level,” by Richard Goering, SCDsource Newsletter, March 2008.
- “Winners & Losers 2007: Beauty and the Beast - Not Ready to Wear,” by Harry Goldstein, IEEE Spectrum, Jan. 2007.
- “Electronic Garments Sense Emotion,” by Tracy Schrader, Discovery News, Oct. 2006.
- “Clothing Goes Hi-Tech,” by Nicole McEwen, The Eagle Tribune, Dec. 2005.
- “Wearing Wires,” by Malcolm Beith, Newsweek International, July 2003.
- “Tomorrow’s technology points to present-day solutions,” by Nicholas Mokhoff, EE Times, June 2002.

## **Professional Activities**

### **Governing Boards**

- Chair, ECE Graduate Studies Committee, 2011-present.
- Member, CMU Faculty Review Committee, 2011-present.
- Member, CMU Faculty Senate Nominating Committee, 2010-present.
- Member, SRC Undergraduate Research Opportunities Selection Committee, 2009-present.
- Member, CMU University-level Non-Tenure Promotions Committee, 2009-present.
- Awards Chair, Special Interest Group on Design Automation, Association for Computing Machinery (ACM-SIGDA), 2009-present.
- Member, CMU Faculty Senate, 2007-2011.
- Secretary, Executive Committee of the SIG Governing Board (SGB) of the Association for Computing Machinery (ACM), 2007-2010.
- Chair-Elect, Special Interest Group on Design Automation, Association for Computing Machinery (ACM-SIGDA), 2005-2009.
- Vice-Chair for Special Interest Group (SIG) Development, Executive Committee of the SIG Governing Board (SGB) of the Association for Computing Machinery (ACM), 2006-2007.
- Member, ACM Awards Committee (Outstanding Contributions to ACM Award Subcommittee), 2007-2010.

### **Editorships**

- Guest Editor, *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, Special Issue on Parallel CAD, 2011.
- Associate Editor, *ACM Transactions on Design Automation of Electronic Systems*, 2010-present.
- Associate Editor, *IEEE Transaction on VLSI Systems*, 2005-2011.
- Guest Editor, *IEEE Transaction on VLSI Systems*, Special Section on Low Power Electronics and Design, 2007.
- Editor-in-Chief, *ACM/SIGDA Newsletter*, 2002-2005.
- Guest Editor, *IEEE MICRO Magazine*, Special Issue on Power and Complexity Aware Design, Oct. 2003.

### **Conference Committees, Boards, and Panel Reviews**

- NSF Panel Reviewer, 2000-present.
- Technical Program Chair, *IEEE/ACM Intl. Symposium on Networks-on-Chip*, 2012.
- Finance Chair, *IEEE/ACM Intl. Symposium on Networks-on-Chip*, 2011.
- ACM/SIGDA Representative, *IEEE/ACM Design, Automation, and Test in Europe Conference*, 2009-present.

- Member, Executive Committee, *ACM/IEEE Design Automation Conference*, 2005-2009.
- General Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2007.
- Technical Program Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2006.
- Exhibits Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design*, 2001-2005.
- Technical Program Chair, *ACM/IEEE International Workshop on Logic and Synthesis*, 2004.
- General Chair, *ACM/IEEE International Workshop on Logic and Synthesis*, 2003.
- Chair, Organizing Committee, *SIGDA Ph.D. Forum at Design Automation Conference*, 2002-2003.
- Panel Chair, *ACM/IEEE International Workshop on Logic and Synthesis*, 2001-2002.
- Panel Chair, *IEEE Computer Society Intl. Symposium on VLSI*, 2002-2004.
- Publicity Chair, *IEEE Computer Society Annual Workshop on VLSI*, 2001.

#### **Technical Program Committees – Conferences and Symposia**

- Member, Technical Program Committee, *ACM/IEEE Intl. Conference on Computer-Aided Design*, 2011-present, 2007-2008 and 2001-2003.
- Member, Technical Program Committee, *ACM/IEEE Intl. Symposium on Low Power Electronics and Design*, 2011-present, 2002-2005.
- Member, Technical Program Committee, *IEEE/ACM Intl. Symposium on Networks on Chip*, 2010-2011.
- Member, Technical Program Committee, *IEEE Design, Automation and Test in Europe Conference*, 2012, 2010, 2001-2003.
- Member, Technical Program Committee, *ACM Intl. Symposium on Computer Architecture*, 2009, 2004.
- Member, Technical Program Committee, *ACM/IEEE Design Automation Conference*, 2005-2008.
- Member, Technical Program Committee, *ACM/IEEE Intl. Symp. on Microarchitecture*, 2006, 2008.
- Member, Technical Program Committee, *IEEE Asian-South Pacific Design Automation Conference*, 2006-2007.
- Member, Technical Program Committee, *Intl. Symposium on Asynchronous Circuits and Systems*, 2007, 2004-2005.
- Member, Technical Program Committee, *Intl. Symp. on High Performance Computer Architecture*, 2005.
- Member, Technical Program Committee, *Intl. Symposium on Circuits and Systems*, 2004.
- Member, Technical Program Committee, *IEEE Intl. Conference on Computer Design*, 2002-2003.
- Member, Organizing Committee, *SIGDA Ph.D. Forum at Design Automation Conference*, 2001-2003.

#### **Workshop Committees and Boards**

- Chair, *CRA-W/CDC Workshop on Diversity in Design Automation and Test*, 2011.
- Technical Program Co-Chair, *Workshop on Micro Power Management for Macro Systems on Chip*, in conjunction with *Design, Automation and Test in Europe Conference*, 2011.
- Technical Program Co-Chair, *Workshop on Complexity Effective Design*, in conjunction with *International Symposium on Computer Architecture*, 2002-2006.
- Member, Organizing Committee, *Ph.D. Forum, Grace Hopper Celebration of Women in Computing*, 2004.
- Technical Program Co-Chair, *Workshop on Compilers and Operating Systems on Low Power*, in conjunction with *IEEE Conference on Parallel Architectures and Compiling Technologies*, 2002-2003.
- Technical Program Co-Chair, *Workshop on Modeling, Analysis and Middleware Support for Electronic Textiles*, in conjunction with *International Conference on Architectural Support for Programming Languages and Operating Systems*, 2002.

### Technical Program Committees – Workshops

- Member, Technical Program Committee of *ACM/IEEE International Workshop on Logic Synthesis, 1999-2006*.
- Member, Technical Program Committee of the *Power Aware Computer Systems Workshop (in conjunction with ASPLOS or MICRO), 2000, 2003-2004*.
- Member, Technical Program Committee of the *Formal Methods for GALS Systems Workshop (in conjunction with FME), 2003*.
- Member, Technical Program Committee, *Workshop on Compilers and Operating Systems on Low Power*, in conjunction with *IEEE Conference on Parallel Architectures and Compiling Technologies, 2001*.

### Reviewing Activities

- *IEEE Trans. on Computers, IEEE Trans. on Computer-Aided Design of Integrated Circuits, IEEE Trans. on VLSI Systems, IEEE Trans. on Circuits and Systems II, IEEE Micro, ACM Trans. on Design Automation of Electronic Systems, ACM Trans. on Embedded Computing Systems, Foundations and Trends in EDA, Journal of System Architecture, ACM/IEEE Design Automation Conference, IEEE/ACM International Conference on Computer-Aided Design, ACM/IEEE International Symposium on Low-Power Electronics and Design, IEEE International Symposium on Circuits and Systems, IEEE International Conference on Computer Design, ACM/IEEE International Workshop on Logic Synthesis.*

### Technical Societies

- Senior Member, *Institute of Electrical and Electronics Engineers* and *Association for Computing Machinery* (since 2009)
- Member of *IEEE-Circuits and Systems Society* and *IEEE-Computer Society* (since 1994)
- Member of *ACM-Special Interest Group on Design Automation* (since 1997)
- Member of *ACM-Special Interest Group on Computer Architecture* (since 2001)
- Member of *ACM-Special Interest Group on Microarchitecture* (since 2005)

## Publications

### Books and Book Chapters

[B8] S. Herbert, D. Marculescu, “Variability-Aware Frequency Scaling in Multi-Clock Processors,” in *Adaptive and Dynamic Techniques for Processor Optimization: Theory and Practice*, A. Wang and S. Naffziger (eds.), Springer Verlag, 2008.

[B7] E. Talpes, D. Marculescu, “Low power microarchitecture techniques,” in *The VLSI Handbook*, W.-K. Chen (ed.), CRC Book Press, 2006.

[B6] P. Stanley-Marbell, D. Marculescu, R. Marculescu, and P.K. Khosla, “Challenges and Opportunities in Modeling, Analysis and Optimization of Electronic Textiles,” in *Low Power Electronics Design*, C. Piguet (ed.), CRC Book Press, 2004.

[B5] P. Stanley-Marbell, N.H. Zamora, D. Marculescu, R. Marculescu, “Fault-tolerant techniques for ambient intelligent distributed systems,” in *Ambient Intelligence: Impact on embedded-system design*, T. Basten, M. Geilen, H. de Groot (eds.), Kluwer Academic Publishers, 2003.

[B4] V.S.P. Rapaka, D. Marculescu, “Efficient power/performance analysis of embedded and general purpose software applications,” in *Embedded Software for SoC*, A. Jerraya, S. Yoo, N. Wehn, D. Verkest (eds.), Kluwer Academic Publishers, 2003.

[B3] S.W. Haga, N. Reeves, R. Barua, D. Marculescu, “Dynamic functional units assignment for low power,” in *Embedded Software for SoC*, A. Jerraya, S. Yoo, N. Wehn, D. Verkest (eds.), Kluwer Academic Publishers, 2003.

[B2] D. Marculescu, R. Marculescu, "System and microarchitectural level power modeling, optimization, and their implications in energy aware computing," in *Power Aware Design Methodologies*, M. Pedram, J. Rabaey (eds.), Kluwer Academic Publishers, 2002.

[B1] I. Athanasiu, D. (Raiciu) Marculescu, R. Sion, I. Mocanu, "Formal Languages – Applications," Computer Science Department, "Politehnica" University of Bucharest Press, December 1999.

### Archival Journal Papers

[J31] S. Garg, D. Marculescu, "Manufacturing Process Variability-Aware Low Power Embedded Systems Design," under review, *Trans. on Industrial Informatics* (Special Issue on Power-Aware Design for Embedded Systems), submitted 2011.

[J30] S. Garg, D. Marculescu, "Mitigating the Impact of Process Variations on the Performance 3D ICs," under review, *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, submitted 2011.

[J29] K.-C. Wu, D. Marculescu, "A Low-Cost, Systematic Methodology for Soft Error Robustness of Logic Circuits," under review, *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, submitted 2011.

[J28] S. Garg, D. Marculescu, R. Marculescu, "Technology-driven Limits on Run-time Power Management Algorithms for Multi-processor Systems on Chip," in press, *ACM Journal on Emerging Technologies in Computing Systems*, 2011.

[J27] S. Garg, D. Marculescu, "System-Level Leakage Variability Mitigation for MPSoC Platforms Using Body-Bias Islands," in press, *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, 2011.

[J26] S. Herbert, S. Garg, D. Marculescu, "Exploiting Process Variability in Voltage/Frequency Control," in press, *IEEE Trans. on Very Large Scale Integrated (VLSI) Circuits*, 2011.

[J25] S. Garg, D. Marculescu, "On the Impact of Manufacturing Process Variations on the Lifetime of Sensor Networks," in press, *ACM Trans. on Embedded Computing Systems*, 2011.

[J24] N. Miskov-Zivanov, D. Marculescu, "Multiple Transient Faults in Combinational and Sequential Circuits: A Systematic Approach," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.29, no.10, pp.1614-1627, Oct. 2010.

[J23] S. Herbert, D. Marculescu, "Mitigating the Impact of Variability on Chip-Multiprocessor Power and Performance," in *IEEE Trans. on VLSI Systems*, vol.17, no.10, pp.1520-1533, Oct. 2009.

[J22] U.Y. Ogras, R. Marculescu, D. Marculescu, E.-G. Jung, "Design and Management of Voltage-Frequency Island Partitioned Networks-on-Chip," in *IEEE Trans. on VLSI Systems*, vol.17, no.3, pp. 330-341, March 2009. (Special Section on Networks-on-Chip; **Best Paper Award**)

[J21] P. Choudhary, D. Marculescu, "Power Management of Voltage/Frequency Island-Based Systems Using Hardware Based Methods," in *IEEE Trans. on VLSI Systems*, vol.17, no.3, pp. 427-438, March 2009.

[J20] S. Garg, D. Marculescu, "System Level Throughput Analysis for Process Variation Adaptive Multiple Voltage-Frequency Island Designs," in *ACM Trans. on Design Automation of Electronic Systems*, vol.13, No.4, pp. 1-25, Sept. 2008.

[J19] N. Miskov-Zivanov, D. Marculescu, "Modeling and Optimization for Soft Error Reliability of Sequential Circuits," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.27, No.5, pp. 803-816, May 2008.

[J18] D. Marculescu, S. Garg, "Process-Driven Variability Analysis for Single and Multiple Voltage-Frequency Island, Latency-Constrained Systems," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.27, No.5, pp. 893-905, May 2008.

- [J17] U.Y. Ogras, R. Marculescu, H.G. Lee, P. Choudhary, D. Marculescu, M. Kaufman, P. Nelson, "Challenges and Promising Results in NoC Prototyping Using FPGAS," in *IEEE Micro*, vol.27, No.5, Sept-Oct. 2007.
- [J16] R.I. Bahar, D. Hammerstrom, J. Harlow, W.H. Joyner Jr., C. Lau, D. Marculescu, A. Orailoglu, M. Pedram, "Architectures for Silicon Nanoelectronics and Beyond," in *IEEE Computer*, vol. 40, No.1, pp.25-33, Jan. 2007.
- [J15] N. Miskov-Zivanov, D. Marculescu, "Circuit Reliability Analysis Using Symbolic Techniques," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.25, No.12, pp. 2638-2649, Dec. 2006.
- [J14] D. Marculescu, E. Talpes, "Energy Awareness and Uncertainty in Design at Microarchitecture Level," in *IEEE Micro*, vol.25, No.5, pp.64-76, Sept.-Oct. 2005.
- [J13] P. Koopman, H. Choset, R. Gandhi, B. Krogh, D. Marculescu, P. Narasimhan, J.M. Paul, R. Rajkumar, D. Siewiorek, A. Smailagic, P. Steenkiste, D.E. Thomas, C. Wang, "Undergraduate Embedded System Education at Carnegie Mellon," in *ACM Trans. on Embedded Computer Systems*, vol.4, No.3, pp.500-528, Aug. 2005.
- [J12] E. Talpes, D. Marculescu, "Toward a Multiple Clock/Voltage Island Design Style for Power Aware Processors," in *IEEE Trans. on VLSI Systems*, vol.13, No.5, pp.591-603, May 2005.
- [J11] S.W. Haga, N. Reeves, R. Barua, and D. Marculescu, "Dynamic Functional Unit Assignment for Low Power," in *Journal of Supercomputing*, vol.31, No.1, pp. 47-62, Kluwer Academic Publishers, Jan. 2005.
- [J10] E. Talpes, D. Marculescu, "Execution Cache Based Microarchitecture for Power Efficient Superscalar Processors," in *IEEE Trans. on VLSI Systems*, vol.13, No.1, pp.14-26, Jan. 2005.
- [J9] D. Marculescu, R. Marculescu, N. H. Zamora, P. Stanley-Marbell, P. K. Khosla, S. Park, S. Jayaraman, S. Jung, W. Weber, C. Lauterbach, D. Cottet, C. Grzyb, T. Kirstein, G. Troester, M. T. Jones, T. Martin, Z. Nakad, "Electronic Textiles: A Platform for Pervasive Computing," in *Proceedings of the IEEE*, vol.91, No.12, pp. 1995-2018, Dec. 2003.
- [J8] P. Stanley-Marbell, D. Marculescu, R. Marculescu, and P.K. Khosla, "Modeling, Analysis and Self-Management of Electronic Textiles," in *IEEE Trans. on Computers* (Special Issue on Wearable Computing), vol.52, No.8, pp. 996-1010, Aug. 2003.
- [J7] A. Iyer, D. Marculescu, "Microarchitecture Level Power Management," in *IEEE Trans. on VLSI Systems*, vol.10, No.3, pp. 230-239, June 2002.
- [J6] D. Marculescu, R. Marculescu, and M. Pedram, "Theoretical Bounds for Switching Activity Analysis in Finite-State Machines," in *IEEE Trans. on VLSI Systems* (Special Issue on Low Power Design), vol.8, No.3, pp. 335-339, June 2000.
- [J5] D. Marculescu, R. Marculescu, and M. Pedram, "Stochastic Sequential Machines Synthesis with Application to Constrained Sequence Generation," in *ACM Trans. on Design Automation of Electronic Systems*, vol.5, No.2, Jan. 2000.
- [J4] R. Marculescu, D. Marculescu, and M. Pedram, "Sequence Compaction for Power Estimation: Theory and Practice," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.18, No.7, pp. 973-993, 1999.
- [J3] R. Marculescu, D. Marculescu, and M. Pedram, "Probabilistic Modeling of Dependencies During Switching Activity Analysis," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol.17, No.2, pp. 73-83, Feb.1998.

[J2] R. Marculescu, D. Marculescu, and M. Pedram, "Vector Compaction Using Dynamic Markov Models," in *IEICE Trans. on Fundamentals* (Special issue on VLSI design and CAD algorithms), vol. E80-A, No.10, October 1997, Japan.

[J1] D. Marculescu, R. Marculescu, and M. Pedram, "Information Theoretic Measures for Power Analysis," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* (Special Issue on Low Power Design), vol.15, No.6, pp. 599-610, June 1996.

### Peer Reviewed Conference Papers in Published Proceedings<sup>1</sup>

[C78] D.-C. Juan, H. Zhou, D. Marculescu, X. Li, "A Learning-Based Autoregressive Model for Fast Transient Thermal Analysis of Chip-Multiprocessors," in *Proc. IEEE/ACM Asian-South Pacific Design Automation Conference (ASPDAC)*, Sydney, Australia, Jan. 2012.

[C77] Y. L. Chuang, T. Y. Ho, H. T. Lin, Y. W. Chang, D. Marculescu, "PRICE: Power Reduction by Placement and Clock-Network Co-Synthesis for Pulsed-Latch Designs," in *Proc. of the IEEE/ACM Intl. Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, Nov. 2011.

[C76] N. Miskov-Zivanov, A. Bresticker, S. Venkatakrishnan, P. Kashinkunti, D. Krishnaswamy, D. Marculescu, J. Faeder, "Regulatory Network Analysis Acceleration with Reconfigurable Hardware," in *Proc. Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Boston, MA, Sept. 2011.

[C75] K.-C. Wu, D. Marculescu, M.-C. Lee, and S.-C. Chang, "Analysis and Mitigation of NBTI-Induced Performance Degradation for Power-Gated Circuits," in *Proc. of ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Fukuoka, Japan, Aug. 2011.

[C74] N. Miskov-Zivanov, D. Krishnaswamy, S. Venkataraman, A. Bresticker, D. Marculescu, J.R. Faeder, "Emulation of Biological Networks in Reconfigurable Hardware," in *Proc. ACM Intl. Conference on Bioinformatics and Computational Biology (BCB)*, Chicago, IL, Aug. 2011.

[C73] S. Garg, D. Marculescu, "Parametric Yield and Reliability of 3D Integrated Circuits: New Challenges and Solutions," in *Proc. IEEE VLSI Test Symposium (VTS)*, Dana Point, CA, May 2011. **(Invited paper)**

[C72] D.-C. Juan, S. Garg, and D. Marculescu, "Statistical Thermal Evaluation and Mitigation Techniques for 3D Chip-Multiprocessors In the Presence of Process Variations," in *Proc. of IEEE/ACM Design, Automation and Test in Europe (DATE)*, Grenoble, France, March 2011.

[C71] K.-C. Wu and D. Marculescu, "Aging-Aware Timing Analysis and Optimization Considering Path Sensitization," in *Proc. of IEEE/ACM Design, Automation and Test in Europe (DATE)*, Grenoble, France, March 2011.

[C70] S. Garg, D. Marculescu, and S. Herbert, "Process Variation Aware Performance Modeling and Dynamic Power Management for Multicore Systems," in *IEEE/ACM Intl. Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, Nov. 2010. **(Embedded tutorial)**

[C69] S. Garg, D. Marculescu, R. Marculescu, "Custom Feedback Control: Enabling Truly Scalable On-Chip Power Management for MPSoCs," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Austin, TX, Aug. 2010.

[C68] D. Marculescu and N. Miskov-Zivanov, "Formal Modeling and Reasoning for Reliability Analysis," in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2010. **(Invited paper)**

[C67] S. Garg, R. Yan, R. Marculescu, D. Marculescu, U. Schlichtmann, "Architectural Modeling of the Impact of Process Variations on Network-on-Chip Clock Frequency," in *Proc. Workshop on Diagnostic*

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<sup>1</sup> Acceptance rates are 15-30%, with lower rates for more recent years.

*Services in Network-on-Chips (DSNOC)*, in conjunction with *ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2010.

[C66] N. Miskov-Zivanov and D. Marculescu, "Modeling and Analysis of SER in Combinational Circuits," in *Proc. of IEEE Workshop on Silicon Errors in Logic – System Effects (SELSE)*, Stanford, CA, March 2010. **(Invited paper)**

[C65] K.-C. Wu, D. Marculescu, "Clock Skew Scheduling for Soft-Error-Tolerant Sequential Circuits," in *Proc. of IEEE/ACM Design, Automation and Test in Europe (DATE)*, Dresden, Germany, March 2010.

[C64] A. Bonnoit, S. Herbert, D. Marculescu, and L. Pileggi, "Integrating Dynamic Voltage/Frequency Scaling and Adaptive Body Biasing using Test-time Voltage Selection," in *Proc. of ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, San Francisco, CA, Aug. 2009.

[C63] S. Garg, D. Marculescu, R. Marculescu, and U. Ogras, "Technology-driven Limits on DVFS Controllability of Multiple Voltage-Frequency Island Designs," in *Proc. of IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, Jul. 2009.

[C62] K.-C. Wu and D. Marculescu, "Joint Logic Restructuring and Pin Reordering for Mitigating NBTI-Induced Affects," in *Proc. of IEEE/ACM Design, Automation and Test in Europe (DATE)*, Nice, France, Apr. 2009.

[C61] S. Garg and D. Marculescu, "Process Variability Analysis and Mitigation for 3D MPSoCs," in *Proc. of IEEE/ACM Design, Automation and Test in Europe (DATE)*, Nice, France, Apr. 2009. **(Paper nominated for Best Paper Award)**

[C60] S. Garg and D. Marculescu, "3D GCP - An Analytical Model for the Impact of Process Variations on the Critical Path Delay of 3D ICs," in *Proc. of IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, Mar. 2009. **(Best Paper Award)**

[C59] W.-P. Lee, Y.-W. Chang, and D. Marculescu, "Post-Floorplanning Power/Ground Ring Synthesis for Multiple-Supply-Voltage Designs," in *Proc. of ACM International Symposium on Physical Design (ISPD)*, San Diego, CA, Mar. 2009.

[C58] S. Herbert and D. Marculescu, "Variation-Aware Dynamic Voltage/Frequency Scaling," in *Proc. of the 15th International Symposium on High-Performance Computer Architecture (HPCA)*, Raleigh, NC, Feb. 2009.

[C57] K.-C. Wu, D. Marculescu, "Power-Aware Soft Error Hardening via Selective Voltage Scaling," in *Proc. IEEE Intl. Conference on Computer Design (ICCD)*, Lake Tahoe, CA, Oct. 2008. **(Best Paper Award)**

[C56] N. Miskov-Zivanov, K.-C. Wu, D. Marculescu, "Process Variability-Aware Transient Fault Modeling and Analysis," in *Proc. IEEE/ACM Intl. Conference on Computer Aided-Design (ICCAD)*, in San Jose, CA, Nov. 2008.

[C55] S. Garg, D. Marculescu, "System-Level Mitigation of WID Leakage Power Variability Using Body-Bias Islands," in *Proc. ACM/IEEE Intl. Conference on Hardware-Software Codesign and System Synthesis (CODES-ISSS)*, Atlanta, GA, Oct. 2008.

[C54] S. Herbert, D. Marculescu, "Analysis of Variability-Tolerance in Chip-Multiprocessors," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2008. **(Paper nominated for Best Paper Award)**

[C53] U.Y. Ogras, R. Marculescu, D. Marculescu, E.-G. Jung, "Variation-Adaptive Feedback Control for Networks-on-Chip with Multiple Clock Domains," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2008. **(Paper nominated for Best Paper Award)**

- [C52] N. Miskov-Zivanov, D. Marculescu, "A Systematic Approach to Modeling and Analysis of Transient Faults in Logic Circuits," in *Proc. IEEE Intl. Symposium on Quality on Electronic Design (ISQED)*, San Jose, CA, March 2008.
- [C51] K.-C. Wu, D. Marculescu, "Soft Error Rate Reduction Using Redundancy Addition and Removal," in *Proc. IEEE/ACM Asian-South Pacific Design Automation Conference (ASPDAC)*, Seoul, Korea, Jan. 2008.
- [C50] S. Garg, D. Marculescu, "On the Impact of Manufacturing Process Variations On the Lifetime of Sensor Networks," in *Proc. ACM/IEEE Intl. Conference on Hardware-Software Codesign and System Synthesis (CODES-ISSS)*, Salzburg, Austria, Sept. 2007.
- [C49] S. Herbert and D. Marculescu, "Analysis of Dynamic Voltage/Frequency Scaling in Chip-Multiprocessors," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Portland, OR, Aug. 2007.
- [C48] U.Y. Ogras, P. Choudhary, R. Marculescu, D. Marculescu, "Voltage-Frequency Island Partitioning for GALS-Based Networks-on-Chip," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, San Diego, CA, June 2007. (**Paper nominated for Best Paper Award**)
- [C47] S. Garg, D. Marculescu, "System-Level Process Variation Driven Throughput Analysis for Single and Multiple Voltage-Frequency Island Designs," in *Proc. IEEE Design, Automation and Test in Europe (DATE)*, Nice, France, Apr. 2007.
- [C46] N. Miskov-Zivanov, D. Marculescu, "Soft Error Rate Analysis for Sequential Circuits," in *Proc. IEEE Design, Automation and Test in Europe (DATE)*, Nice, France, Apr. 2007.
- [C45] P. Stanley-Marbell, D. Marculescu, "An 0.9 X 1.2", Low Power, Energy-Harvesting System with Custom Multi-Channel Communication Interface," in *Proc. IEEE Design, Automation and Test in Europe (DATE)*, Nice, France, Apr. 2007.
- [C44] N. Miskov-Zivanov, D. Marculescu, "MARS-S: Modeling, Analysis and Reduction of Soft Errors in Sequential Circuits," in *Proc. IEEE Intl. Symposium on Quality in Electronic Design (ISQED)*, San Jose, CA, March 2007. (**Paper nominated for Best Paper Award**)
- [C43] P. Stanley-Marbell, D. Marculescu, "Sunflower: Full-System Embedded Microarchitecture Evaluation," in *Proc. Intl. Conf. on High Performance Embedded Architectures & Compilers (HiPEAC)*, Ghent, Belgium, Jan. 2007.
- [C42] D. Marculescu, S. Garg, "System-Level Process-Driven Variability Analysis for Single and Multiple Voltage-Frequency Island Systems," in *Proc. IEEE/ACM Intl. Conference on Computer Aided-Design (ICCAD)*, in San Jose, CA, Nov. 2006.
- [C41] P. Choudhary, D. Marculescu, "Hardware based Frequency/Voltage Control of Voltage Frequency Island Systems," in *Proc. IEEE/ACM Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, Seoul, Korea, Oct. 2006.
- [C40] N. Miskov-Zivanov, D. Marculescu, "MARS-C: Modeling, Analysis and Reduction of Soft Errors in Combinational Circuits," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 2006.
- [C39] C.-H. Chang, D. Marculescu, "Design and Analysis of a Low Power VLIW DSP Core," in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Karlsruhe, Germany, March 2006.
- [C38] K. Niyogi, D. Marculescu, "System Level Power and Performance Modeling of GALS Point-to-point Communication Interfaces," in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, San Diego, CA, Aug. 2005.

- [C37] D. Marculescu, E. Talpes, “Variability and Energy Awareness: A Microarchitecture-Level Perspective,” in *ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2005.
- [C36] E. Talpes, D. Marculescu, “Increased Scalability and Power Efficiency through Multiple Speed Pipelines,” in *Proc. ACM Intl. Symposium on Computer Architecture (ISCA)*, Madison, WI, June 2005.
- [C35] D. Marculescu, “Energy Bounds for Fault-Tolerant Nanoscale Designs,” in *Proc. IEEE Design, Automation and Test in Europe (DATE)*, Munich, Germany, March 2005. (**Paper nominated for Best Paper Award**)
- [C34] K. Niyogi and D. Marculescu, “Speed and Voltage Selection for GALS Systems Based on Voltage/Frequency Islands,” in *IEEE/ACM Asian-South Pacific Design Automation Conference (ASPDAC)*, Shanghai, China, Jan. 2005. (**Best Paper Award**)
- [C33] R. Marculescu, D. Marculescu, and L. Pileggi, “Toward an Integrated Design Methodology for Fault-Tolerant, Multiple Clock/Voltage Integrated Systems,” in *Proc. IEEE Intl. Conference on Computer Design (ICCD)*, San Jose, CA, October 2004. (**Invited paper**)
- [C32] D. Marculescu, “Application Adaptive Energy Efficient Clustered Architectures,” in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Newport Beach, CA, Aug. 2004.
- [C31] E. Talpes and D. Marculescu, “Impact of Technology Scaling on Energy Aware Execution Cache-based Microarchitectures,” in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Newport Beach, CA, Aug. 2004.
- [C30] P. Stanley-Marbell and D. Marculescu, “Local Decisions and Triggering Mechanisms for Adaptive Fault-Tolerance,” in *Proc. IEEE Design, Automation and Test in Europe Conf. (DATE)*, Paris, France, Feb. 2004.
- [C29] V.S.P. Rapaka, E. Talpes, D. Marculescu, “Mixed-Clock Issue Queue Design for Energy Aware, High-Performance Cores,” in *Proc. IEEE/ACM Asian-South Pacific Design Automation Conference (ASPDAC)*, Yokohama, Japan, Jan. 2004.
- [C28] P. Stanley-Marbell and D. Marculescu, “Dynamic Fault-Tolerance and Metrics for Battery Powered, Failure-Prone Systems,” in *Proc. IEEE/ACM Intl. Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, Nov. 2003.
- [C27] D. Marculescu, N. H. Zamora, P. Stanley-Marbell, R. Marculescu, “Fault-Tolerant Techniques for Ambient Intelligent Distributed Systems,” in *Proc. IEEE/ACM Intl. Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, Nov. 2003.
- [C26] V.S.P. Rapaka and D. Marculescu, “A Mixed-Clock Issue Queue Design for Globally Asynchronous, Locally Synchronous Processor Cores,” in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Seoul, Korea, Aug. 2003.
- [C25] E. Talpes and D. Marculescu, “A Critical Analysis of Application-Adaptive Multiple Clock Processors,” in *Proc. ACM/IEEE Intl. Symposium on Low Power Electronics and Design (ISLPED)*, Seoul, Korea, Aug. 2003.
- [C24] M. Lindwer, D. Marculescu, T. Basten, R. Zimmermann, R. Marculescu, S. Jung, and E. Cantatore, “Ambient Intelligence Visions and Achievements: Linking Abstract Ideas to Real-World Concepts,” in *IEEE Design, Automation and Test in Europe Conf. (DATE)*, Munich, Germany, March 2003. (**Hot topic session**)
- [C23] V.S.P. Rapaka and D. Marculescu, “Pre-characterization Free Efficient Power/Performance Analysis of Embedded and General Purpose Software Applications,” in *Proc. IEEE Design, Automation and Test in Europe Conf. (DATE)*, Munich, Germany, March 2003.

- [C22] S.W. Haga, N. Reeves, R. Barua, and D. Marculescu, "Dynamic Functional Unit Assignment for Low Power," in *Proc. IEEE Design, Automation and Test in Europe Conf. (DATE)*, Munich, Germany, March 2003.
- [C21] A. Iyer and D. Marculescu, "Power Efficiency of Voltage Scaling in Multiple Clock, Multiple Voltage Cores," in *Proc. IEEE/ACM Intl. Conference on Computer Aided Design (ICCAD)*, San Jose, CA, Nov. 2002.
- [C20] D. Marculescu, R. Marculescu, and P. Khosla, "Challenges and Opportunities in E-textile Analysis, Modeling and Optimization," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Anaheim, CA, June 2002. **(Special session)**
- [C19] A. Iyer and D. Marculescu, "Power Performance Evaluation of Globally Asynchronous, Locally Synchronous Processors," in *Proc. IEEE Intl. Symposium on Computer Architecture (ISCA)*, Anchorage, AK, May 2002.
- [C18] R. Marculescu and D. Marculescu, "Is  $Q=MC^2$ ? (On the Relationship between the Model of Colloidal Computing and Quality in Electronic Design)," in *Proc. ACM Intl. Symposium on Quality in Electronic Design (ISQED)*, March 2002. **(Invited paper)**
- [C17] D. Marculescu and A. Iyer, "Application-Driven Processor Design Exploration for Power-Performance Trade-off Analysis," in *Proc. IEEE/ACM Intl. Conference on Computer Aided Design (ICCAD)*, November 2001.
- [C16] E. Talpes and D. Marculescu, "Power Reduction through Work Reuse," in *Proc. ACM Intl. Symposium on Low Power Electronics and Design (ISLPED)*, August 2001.
- [C15] A. Iyer and D. Marculescu, "Power Aware Microarchitecture Resource Scaling," in *Proc. of IEEE Design, Automation and Test in Europe Conf. (DATE)*, Munich, Germany, March 2001.
- [C14] D. Marculescu, "Profile-Driven Code Execution for Low Power Dissipation," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design (ISLPED)*, Rapallo/Portofino Coast, Italy, July 2000.
- [C13] D. Marculescu, R. Marculescu, "Information-Theoretic Bounds for Switching Activity Analysis in Finite-State Machines under Temporally Correlated Inputs," in *Proc. 33rd Asilomar Conference on Signals, Systems, and Computers (ASILOMAR)*, October 1999. **(Invited paper)**
- [C12] R. Marculescu, D. Marculescu, and M. Pedram, "Non-Stationary Effects in Trace-Driven Power Analysis," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design (ISLPED)*, San Diego, CA, August 1999.
- [C11] D. Marculescu, R. Marculescu, and M. Pedram, "Theoretical Bounds for Switching Activity Analysis in Finite-State Machines," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design (ISLPED)*, Monterey, CA, August 1998.
- [C10] D. Marculescu, R. Marculescu, and M. Pedram, "Trace-Driven Steady-State Probability Estimation in FSMs with Application to Power Estimation," in *Proc. ACM Design, Automation and Test in Europe Conf. (DATE)*, Paris, France, February 1998.
- [C9] R. Marculescu, D. Marculescu, and M. Pedram, "Block Entropy and High-Order Temporal Effects in Composite Sequence Compaction for Finite-State Machines," in *Proc. ACM Intl. Symp. on Low Power Electronics and Design (ISLPED)*, Monterey, CA, August 1997.
- [C8] R. Marculescu, D. Marculescu, and M. Pedram, "Hierarchical Sequence Compaction for Power Estimation," in *Proc. ACM/IEEE Design Automation Conf. (DAC)*, Anaheim, CA, June 1997. **(Paper nominated for Best Paper Award)**
- [C7] D. Marculescu, R. Marculescu, and M. Pedram, "Sequence Compaction for Probabilistic Analysis of Finite-State Machines," in *Proc. ACM/IEEE Design Automation Conf. (DAC)*, Anaheim, CA, June 1997.

[C6] R. Marculescu, D. Marculescu, and M. Pedram, "Adaptive Models for Input Data Compaction for Power Simulators," in *Proc. ACM Asia and South-Pacific Design Automation Conf. (ASPDAC)*, Japan, January 1997.

[C5] D. Marculescu, R. Marculescu, and M. Pedram, "Stochastic Sequential Machine Synthesis Targeting Constrained Sequence Generation," in *Proc. ACM/IEEE Design Automation Conf. (DAC)*, Las Vegas, NV, June 1996. (**Paper Nominated for Best Paper Award**)

[C4] C.-Y. Tsui, R. Marculescu, D. Marculescu, and M. Pedram, "Reducing the Run-Time of Simulation-Based Power Estimation by Vector Compaction," in *Proc. ACM/IEEE Design Automation Conf. (DAC)*, Las Vegas, NV, June 1996.

[C3] D. Marculescu, R. Marculescu, and M. Pedram, "Information Theoretic Measures for Energy Consumption at Register Transfer Level," in *Proc. ACM Intl. Symposium. on Low Power Design (ISLPED)*, Dana Point, CA, April 1995.

[C2] R. Marculescu, D. Marculescu, and M. Pedram, "Efficient Power Estimation for Highly Correlated Input Streams," in *Proc. of ACM/IEEE Design Automation Conf. (DAC)*, San Francisco, CA, June 1995.

[C1] R. Marculescu, D. Marculescu, and M. Pedram, "Switching Activity Analysis Considering Spatiotemporal Correlations," in *Proc. IEEE/ACM Intl. Conf. on Computer Aided Design (ICCAD)*, San Jose, CA, November 1994.

#### **Peer Reviewed Workshop Papers, Posters or Demos without Published Proceedings**

[W16] N. Miskov-Zivanov, A. Bresticker, D. Krishnaswamy, S. Venkatakrisnan, D. Marculescu and J. Faeder, "Biological Network Emulation in FPGA," in *Intl. Workshop on Bio-Design Automation (IWBD)*, San Diego, CA, June 2011.

[W15] M.-C. Lee, Y. Shi, Y.-G. Chen, S.-C. Chang and D. Marculescu, "Efficient Wake-Up Scheduling for Multi-Core Systems," in *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Santa Barbara, CA, April 2011.

[W14] N. Miskov-Zivanov, D. Krishnaswamy, S. Venkataraman, A. Bresticker, D. Marculescu, J.R. Faeder, "Emulation of Biological Networks in Reconfigurable Hardware," in *CSHL, Computational Biology*, Cold Spring Harbor, NY, April 2011.

[W13] P. Stanley-Marbell, D. Marculescu, "A Programming Model and Language Implementation for Concurrent Failure-Prone Hardware," in *Workshop on Programming Models for Ubiquitous Parallelism (PMUP)*, in conjunction with *ACM/IEEE Intl. Conf. on Parallel Architectures and Compilation Techniques (PACT)*, Oct. 2006.

[W12] P. Stanley-Marbell and D. Marculescu, "Full-System Simulation for Sensor Networks," in *ACM Conference on Embedded Networked Sensor Systems (SenSys)*, San Diego, Nov. 2005. (demo)

[W11] P. Stanley-Marbell and D. Marculescu, "Cycle-Accurate Full-System Simulation for Sensor Networks," in *Intl. Conference on Mobile Systems, Applications, and Services (MobiSys)*, Seattle, June 2005. (demo)

[W10] N. Miskov-Zivanov and D. Marculescu, "Circuit Reliability Analysis Using Symbolic Techniques," in *IEEE/ACM Intl. Workshop on Logic and Synthesis (IWLS)*, Lake Arrowhead, CA, June 2005.

[W9] S. Hassoun and D. Marculescu, "Toward GALS Design Methodologies," in *Workshop on Formal Methods for GALS Design (FMGALS)*, in conjunction with *Formal Methods in Europe Conference (FME)*, Pisa, Italy, Sep. 2003.

[W8] P. Stanley-Marbell and D. Marculescu, "Programming Crystalline Hardware," in *Workshop on Non-Silicon Computing (NSC)*, in conjunction with *Intl. Symp. on Computer Architecture (ISCA)*, San Diego, June 2003.

[W7] P. Stanley-Marbell and D. Marculescu, "Dynamic Fault-Tolerance Management in Failure-Prone and Battery-Powered Systems," in *IEEE/ACM Intl. Workshop on Logic and Synthesis (IWLS)*, Laguna Beach, CA, May 2003.

[W6] N.H. Zamora, P. Stanley-Marbell, R. Marculescu, D. Marculescu, "PreCopying: An Improved Code Migration Technique for Future Fault-Tolerant Electronic Textiles," in *Proc. Workshop on Modeling, Analysis and Middleware Support for Electronic Textiles (MAMSET)*, in conjunction with *ACM Intl. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, San Jose, CA, Oct. 2002.

[W5] D. Marculescu, R. Marculescu, and P. Khosla, "Challenges and Opportunities in E-textile Analysis, Modeling and Optimization," in *International Conference on Interactive Textiles for the Warrior*, Boston, MA, July 2002. **(Invited poster)**

[W4] A. Iyer and D. Marculescu, "Run-time Scaling of Microarchitecture Resources in a Processor for Energy Savings," in *Proc. KoolChips Workshop (KOOL)*, in conjunction with *International Symposium on Microarchitecture (MICRO)*, Monterey, Dec. 2000.

[W3] D. Marculescu, "Power Efficient Processors Using Multiple Supply Voltages," in *Proc. Workshop on Compilers and Operating Systems for Low Power (COLP)*, in conjunction with *International Conference on Parallel Architectures and Compilation Techniques (PACT)*, Philadelphia, Oct. 2000.

[W2] D. Marculescu, "On the Use of Microarchitecture-Driven Dynamic Voltage Scaling," in *Proc. Workshop on Complexity-Effective Design (WCED)*, in conjunction with *Intl. Symp. on Computer Architecture (ISCA)*, Vancouver, BC, June 2000.

[W1] D. Marculescu, R. Marculescu, and M. Pedram, "High-Order Temporal Effects in Finite State Machine Analysis," in *Intl. Workshop. on Logic Synthesis (IWLS)*, Lake Tahoe, CA, May 1997.

## **Professional Magazines and Review Articles**

[PM4] D. Marculescu, J. Henkel, "Guest Editors' introduction: Special section on low power electronics and design," in *IEEE Trans on VLSI Systems*, 2008.

[PM3] D. Marculescu, R. Marculescu, S. Park, S. Jayaraman, "Ready to Ware," in *IEEE Spectrum*, vol.40, no.10, pp. 28-32, Dec. 2003.

[PM2] P. Bose, D.H. Albonesi, D. Marculescu, "Guest editors' introduction: Power and complexity aware design," in *IEEE Micro*, vol.23, no.5, pp. 8-11, Sept.-Oct. 2003.

[PM1] D. Marculescu, "E-textiles: toward computational clothing," in *IEEE Pervasive Computing*, vol.2, no.1, pp. 89-95, Jan-Mar. 2003.

## **Invited Tutorials, Panels, Talks, and Lectures<sup>2</sup>**

[TL54] "Energy Aware Computing: Beyond the "Silicon Box"," Bell Labs @ CMU Workshop, Pittsburgh, PA, Sept. 2011.

[TL53] "Process Variation Aware Performance Modeling and Dynamic Power Management for Multi-Core Systems," University College Cork, Ireland, July 2011.

[TL52] "Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems," keynote speech, Design Reliability and Variability Workshop (DRVW), in conjunction with IEEE VLSI Test Symposium (VTS), Dana Point, CA, June 2011.

[TL51] "Cost-Effective, "Just-in-Logic" Aging-Aware Fault Detection, Isolation, and Repair," Cisco, October 2010.

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<sup>2</sup> Not including research review talks.

- [TL50] “Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems,” SanDisk, September 2010.
- [TL52] “Process Variation-Aware 3D Thermal Modeling and Management for NoC Designs,” CEA-LETI, July 2010.
- [TL51] “Aging Modeling and Optimization in Digital Systems,” CEA-LETI, July 2010.
- [TL51] “Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems,” Universite Joseph Fourier, July 2010.
- [TL50] “Process Variation Aware Performance Modeling and Dynamic Power Management for Multi-Core Systems,” Universite Joseph Fourier, July 2010.
- [TL49] “Symbolic Reliability Modeling, Analysis, and Optimization of Digital Systems,” Cisco, May 2010 and June 2010.
- [TL48] “Multi-domain Processors: Challenges, Design Methods, and Recent Developments,” (with R. Marculescu, R. Ginosar, S. Rusu), half-day tutorial at International Symposium on Computer Architecture, St. Malo, France, June 2010.
- [TL47] “Process Variation-Aware Dynamic Power Management for Multi-Core Systems,” Intel Corp., Oct. 2009.
- [TL46] “System Level Process Variation Modeling and Mitigation,” Dept. of Computer Science, Universitat Politècnica de Catalunya, Barcelona, Spain, July 2009.
- [TL45] “System Level Process Variation Modeling and Mitigation,” Technische Universitaet Muenchen, Germany, June 2009.
- [TL44] “System Level Process Variation Modeling and Mitigation,” Dept. of Computer Science, Universidad Complutense de Madrid, Madrid, Spain, April 2009.
- [TL43] “DFM Revisited: A Comprehensive Analysis of Variability at all Levels of Abstraction,” (with Lars Liebman, Praveen Elakkumanan, Puneet Gupta, Dureseti Chidambarao, Nagesh Tamarapalli), full-day tutorial at Design Automation Conference, Anaheim, CA, June 2008.
- [TL42] “Design Variability: Challenges and Solutions at Microarchitecture-Architecture Level,” (with Sani Nassif) half-day tutorial at Design, Automation, and Test in Europe Conference, Munich, Germany, March 2008.
- [TL41] “System Level Process Variation Modeling and Mitigation,” Dept. of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Feb. 2008.
- [TL40] “Tutorial on The Sunflower Toolsuite,” (with Phillip Stanley-Marbell), full-day tutorial at Intl. Conf. on High Performance Embedded Architectures & Compilers, Gotteborg, Sweden, Jan. 2008.
- [TL39] “Power Analysis and Optimization of Voltage-Frequency Island Based Designs,” Technology Transfer E-Workshop, Semiconductor Research Corporation, Jan. 2007.
- [TL38] “Circuit and Fabrication Issues for Computer Architects (Traveling from Kansas to Oz),” panelist at the CRA-W/CDC Computer Architecture Workshop, Princeton University, Princeton, NJ, July 2006.
- [TL37] “Analysis and Optimization of Voltage/Frequency-Island Based Designs,” Texas Instruments, April 2006.
- [TL36] “High-Level Power Analysis and Optimization,” Intel Corp., January 2006.
- [TL35] “Energy Awareness and Uncertainty in Design at Microarchitecture Level,” Intel Labs, Pittsburgh, PA, October 2005.

- [TL34] “Energy Awareness and Uncertainty in Design at Microarchitecture Level,” Dept. of Electrical and Computer Engineering, Delft University, Delft, Netherlands, July 2005.
- [TL33] “Power Analysis and Optimization of Voltage/Frequency-Island Based Designs,” Semiconductor Research Corporation, Integrated Systems Kick-Off Meeting, May 2005.
- [TL32] “Energy Awareness and Uncertainty in Design at Microarchitecture Level,” Dept. of Computer Science, Stanford University, Stanford, CA, May 2005.
- [TL31] “Energy Awareness and Uncertainty in Design at Microarchitecture Level,” Dept. of Electrical and Computer Engineering, University of Texas, Austin, TX, March 2005.
- [TL30] “Energy Awareness and Uncertainty in Design at Microarchitecture Level,” Austin Conference on Energy Efficient Design (ACEED), IBM Research, Austin, TX, March 2005.
- [TL29] “Enabling Energy Awareness in Emerging Platforms,” keynote speech at SoC Technology Center, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, Oct. 2004.
- [TL28] “Energy Modeling and Optimization at Microarchitecture and System Level,” tutorial at SoC Technology Center, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, Oct. 2004.
- [TL27] “Toward an Integrated Design Methodology for Fault-Tolerant, Multiple Clock/Voltage Integrated Systems,” IEEE Intl. Conference on Computer Design (ICCD), San Jose, CA, Oct. 2004.
- [TL26] “Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems,” Dept. of Computer Science, Karlsruhe University, Karlsruhe, Germany, Apr. 2004.
- [TL25] “Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems,” Dept. of Electrical Engineering, Princeton University, Princeton, NJ, Apr. 2004.
- [TL24] “Energy Aware Computing: Synchronous vs. Partially Asynchronous Processors,” IBM Research T.J. Watson, Apr. 2004.
- [TL23] “Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems,” Electronic System Design Seminar, University of California, Berkeley, CA, Nov. 2003.
- [TL22] “Dynamic Power and Fault Tolerance for Ambient Intelligent Distributed Systems,” Information Sciences and Technology Seminar, California Institute of Technology, Pasadena, CA, Oct. 2003.
- [TL21] “IEEE Spectrum Panel: Applying Sensor Networks Into Wearable Fabrics,” panel at Intel Developer Forum, San Jose, CA, Oct. 2003.
- [TL20] “Current Trends and Issues in Energy Aware Computing Systems,” lecture at European Summer School on Embedded Systems, Vasteras, Sweden, July 2003.
- [TL19] “Partially asynchronous microprocessor design,” (with Dave Albonesi and Pradip Bose), half-day tutorial at International Symposium on Computer Architecture, in conjunction with Federated Computing Research Conference, (FCRC-ISCA), San Diego, CA, June 2003.
- [TL18] “Partially asynchronous microprocessor design,” (with Dave Albonesi and Pradip Bose), half-day tutorial at International Symposium on Microarchitecture (MICRO), Istanbul, Turkey, November 2002.
- [TL17] “Energy Aware Computing: Synchronous vs. Partially Asynchronous Processors,” Intel’s Low Power Research Symposium, Sept. 2002.
- [TL16] “Minimally clocked microprocessor design,” (with Dave Albonesi and Pradip Bose), half-day tutorial at International Conference on Supercomputing, New York, June 2002.
- [TL15] “Challenges and Opportunities in E-textile Analysis, Modeling and Optimization,” special session at ACM/IEEE Design Automation Conference (DAC), Anaheim, CA, June 2002.

[TL14] “Power and Performance Evaluation of Globally Asynchronous, Locally Synchronous Processors,” Intel Corp., April 2002.

[TL13] “High-Level Power Modeling and Optimization,” lecture at ACM-SIGDA Design Automation Summer School, Cape Cod, MA, May 2001

[TL12-10] “Challenges in energy aware computing,” Intel's Low Power Research Symposium, as well as Compaq WRL and HP Labs, November 2000.

[TL9] “Power Modeling and Optimization of High-Performance Systems,” Carnegie Mellon University, Pittsburgh, PA, Jan. 2000.

[TL8] “Information-Theoretic Bounds for Switching Activity Analysis in Finite-State Machines under Temporally Correlated Inputs,” 33<sup>rd</sup> Asilomar Conference on Signals, Systems, and Computers (ASILOMAR), October 1999.

[TL7] “Power Modeling and Optimization of High-Performance Systems,” University of Minnesota, Minneapolis, MN, Dec. 1999.

[TL6] “The Synthesis of Power Manageable Hardware: A Case Study,” University of Maryland, College Park, MD, March 1999.

[TL5] “Power Analysis and Optimization of Digital Circuits,” University of Maryland, Computer Engineering Seminar Series, College Park, MD, Dec. 1998.

[TL4-1] “Power Analysis and Optimization of Digital Circuits,” Carnegie Mellon University, Pittsburgh, PA, May 1998 (also at University of Maryland, College Park, MD; University of Rochester, Rochester, NY; Northwestern University, Evanston, IL; Feb.-May 1998).

## **Outreach and Mentorship**

[M13] First CRA-W/CDC Workshop on Diversity in Design Automation and Test, founder and organizer, Pittsburgh, PA, May 2011.

[M12] “Being A College Professor: The Good, The Bad, and The Ugly,” presenter at the Career Fair, Dorseyville Middle School, Fox Chapel Area School District, Pittsburgh, PA, May 2010.

[M11] “Soft-Error Analysis Using HSPICE,” project advisor and mentor for Sunny Atluri, CMU CIT freshman, as part of Intel First Year Research Experience (IFYRE) program for minority and female engineering students, Aug.2006-Aug.2007.

[M10] “About Low Power Research (and not only!),” invited talk at Women in ECE (WinECE) Fall Dinner, Sept. 2006.

[M9] “Circuit and Fabrication Issues for Computer Architects (Traveling from Kansas to Oz),” panelist at the CRA-W/CDC Computer Architecture Workshop, Princeton University, Princeton, NJ, July 2006.

[M8] “Symbolic Analysis of Circuit Reliability,” project advisor and mentor for Amanda Rainer (Harvey Mudd College), as part of Distributed Mentorship Program, Computing Research Association (CRA), May-Aug. 2005.

[M7] “Impact of Variability on Power and Performance,” project advisor and mentor for Daisy Lee (U.C. California, Berkeley), as part of the Distributed Mentorship Program, Computing Research Association (CRA), May-Aug. 2005.

[M6] “EMG Signal Processing,” project advisor for CMU’s SWE Engineering Your Future, July 2004.

[M5] “Bringing Undergraduates into Your Research Program,” panelist at Computing Research Association Mentorship Workshop, in conjunction with Federated Computing Research Conference, (FCRC-CRA-W), San Diego, CA, June 2003.

[M4] “The Two-Body Problem: Applying for Jobs,” invited panelist, organized by CMU’s Women in SCS, May 2003.

[M3] “The Smart Woman's Job Search in the Academy and Industry,” invited talk at CMU’s Graduate Women Lunch, March 2003.

[M2] “The Academic Environment at Carnegie Mellon and Challenges for International Women,” invited panelist, organized by CMU's Office for International Education, September 2002.

[M1] “Adapting to Advances in Technology: Next Steps Toward Life-Long Learning,” panel moderator and organizer, CRA-W Distinguished Lecture Series, CMU, December 2000.