Switched Capacitor TIA for Parallel Scanning Tunneling Microscope

Scanning Tunneling Microscope (STM) is an instrument for imaging surfaces at the atomic level, which finds tremendous applications in semiconductor physics, microelectronics, and etc. The fact that the amplitude of the tunneling current signal is typically limited to the nanoamp range requires that the front-end TIA provides an ultra-high gain and a low input referred noise. A CMOS Switched-capacitor TIA (SCTIA) is proposed to sense the tunneling current without introducing any large-valued resistors.

The SCTIA is clocked at 166 kHz with three different phases: $\Phi_1$, $\Phi_2$, and $\Phi_3$ (Fig. 1(a)). Fig.1(c) illustrates voltage responses of internal nodes to a sample input current. Charges on $C_1$ and $C_2$ (Fig. 1(b)) are depleted during reset phase $\Phi_1$. After $\Phi_1$ goes low at $t_1$, the input current starts to charge $C_1$ and $v_1$ begins to rise with a slope proportional to the magnitude of input current $i_{in}$. $v_2$ follows the change of $v_1$ after $\Phi_2$ is off at $t_2$. A Sample and Hold (S&H), consisting of a switch $\Phi_3$ and a capacitor $C_3$, samples $v_2$ at the end of $\Phi_3$ and hold the value till next period. A Low Pass Filter (LPF) reconstructs the continuous-time signal from $v_{out}$ and filters out noise outside the band of interest. The SCTIA is measured to achieve a gain as high as 88 MΩ with a 40 kHz bandwidth. CDS reduces the input referred noise current to as low as 25 fA/√Hz (Fig. 2). This SCTIA, integrated with MEMS probes, enables low-noise low-power, sensing of tunneling current in parallel STM application.

Fig. 1: SCTIA (a) clock diagram; (b) schematic; (c) sample voltage response

Fig 2: Measurement and simulation of SCTIA performance: (a) transimpedance gain; (b) noise