

5.4 A 5GHz CMOS Transceiver for IEEE 802.11a Wireless LAN

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High-speed wireless communications at 5GHz, as specified by the IEEE 802.11a Wireless Local Area Network (WLAN) protocol, utilize both channel bandwidths of 20MHz and complex modulation schemes (BPSK, QPSK, 16QAM, and 64QAM) to enable data rates up to 54Mb/s [1]. The radio frequency (RF) and baseband functions for such a system are implemented in a standard 0.25 μ m CMOS technology. The transceiver and a companion baseband chip [2] implement the physical and MAC layers of a 5GHz WLAN system.

Figure 5.4.1 shows a block diagram of the CMOS transceiver, which consists of a transmitter, a receiver, a frequency synthesizer, biasing circuitry, and control logic. Both the transmitter and receiver employ dual conversion with 1GHz intermediate frequency (IF). The transmitter and receiver share the same synthesizer, which generates both the 1GHz and 4GHz local oscillator (LO) signals. Unlike a direct conversion topology, the large frequency separation between the RF and LO frequencies reduces VCO pulling by the on-chip power amplifier (PA). This dual-conversion transceiver architecture avoids off-chip IF filtering by using a high IF. In the receive chain, the choice of a 1GHz IF provides 2GHz frequency separation between the incoming RF signal and its image. As a result, the narrow-band on-chip tuning elements used in the RF and IF gain stages provide -23dBc suppression of the 3GHz image, eliminating the need for an explicit off-chip IF image-reject filter. On the transmit side, the use of image-reject mixers achieves -50dBc suppression of the 3GHz image without additional filtering.

In the transmit chain, modulated analog baseband I and Q input current signals are generated by two 160MHz, 9b current-steering digital-to-analog converters (DACs) on the baseband chip. The fully differential quadrature baseband input currents are mirrored into the 1GHz up-conversion mixer and then up-converted to RF by a pair of 4GHz quadrature mixers. The most challenging aspect of the transmitter design is providing sufficient gain and linear output power for the orthogonal frequency division multiplexing (OFDM) signal, which comprises 52 sub-carriers.

Figure 5.4.2 shows a three-stage class-A power amplifier (PA), wherein each stage consists of a cascoded differential pair. The gates of the cascode transistors are biased at the supply voltage. The cascode topology allows the PA use of a 3.3V supply for increased headroom and improved linearity. On-chip inductors L_{4p} and L_{4n} form parallel resonances with the gate capacitances of output transistors M_{3p} and M_{3n} so that the level-shifting capacitors C_{2p} and C_{2n} can be <2pF. The fully differential PA output reduces the effects of parasitic supply and ground inductances. The inductive loads L_{3p} and L_{3n} are 1.6nH bondwire inductances. Closed-loop power control provides a constant transmitted output power independent of process, temperature, and supply voltage. The power control loop, consisting of a peak detector, a comparator, and 24dB of adjustable transmitter gain in 0.5dB steps, adjusts the transmitter gain until the PA output matches a pre-programmed level. Measurements indicate that the transmitter can provide 22dBm peak output power and

17.8dBm average OFDM output power. Figure 5.4.3 shows a transmitted OFDM spectrum. The measured spectral images and RF carrier leak are -51dBc and -29dBc, respectively.

The receiver mixes the 5GHz RF input first to the 1GHz IF and then to the quadrature baseband outputs for digitization by two 80MHz 9b analog-to-digital converters on the baseband chip. The entire receive chain is designed to provide sufficient dynamic range and linearity for a 64-QAM OFDM signal. The low-noise amplifier (LNA), which consists of a cascoded differential pair as shown in Figure 5.4.4, has 15dB small-signal gain. The inductive degeneration, L_{sp} and L_{sn}, results in a complex input impedance that can be matched to a 50 Ω source impedance with an off-chip matching network. The RF and IF gain stages have 36dB maximum combined gain that significantly reduces the noise contribution of subsequent baseband stages. The down-converted I and Q signals are passed through off-chip passive LC channel-select filters and then amplified by a programmable gain amplifier (PGA). The PGA comprises a cascade of three stages with a composite gain that varies from 0 to 41dB in 1dB steps. Each stage of the PGA consists of a transconductance stage followed by a transresistance stage. The gains of the amplifiers, which are established by resistor ratios, are accurate to within 1dB. The dc offset of the receive chain is cancelled using two pairs of 6b DACs. The dc offset cancellation, automatic gain control, and receive signal strength indicator are implemented by algorithms in the baseband chip. The receiver has 8dB overall receive chain noise figure. The input-referred 1dB compression point is -8.5dBm.

The frequency synthesizer generates the 1GHz and 4GHz LO frequencies needed for the mixers in the receive and transmit chains. As shown in Figure 5.4.1, the synthesizer phase-locks an on-chip VCO to an 8MHz reference. The VCO frequency is determined by p+/n-well varactors. The variable divider in the feedback loop consists of a 16/17 dual-modulus prescaler followed by a divide-by-32 and a channel select decoder. The synthesized frequency can be varied from 4.128GHz to 4.272GHz, which corresponds to an RF carrier frequency ranging from 5.16GHz to 5.34GHz. The quadrature 1GHz LO signals are generated by a divide-by-four counter. Designed in a twisted-ring architecture, this 4GHz divider generates inherently 90° out-of-phase outputs that maintain their relative phase difference over process and temperature. Shown in Figure 5.4.5 is a plot of the frequency synthesizer phase noise as measured at the output of the PA. The overall loop has a bandwidth of 200kHz.

The transceiver is incorporated into a radio system to form a high-speed, IEEE 802.11a-compliant, wireless LAN. Typical measured performance is summarized in Figure 5.4.6. A transceiver die micrograph is shown in Figure 5.4.7. The IC occupies a total die area of 22mm² and is packaged in a 64-pin leadless plastic chip carrier with an exposed backside contact for good thermal and electrical performance.

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References:

- [1] IEEE Standard 802.11a-1999: Wireless LAN MAC and PHY specifications—High-speed physical layer in the 5GHz band, New York: IEEE, 2000.
- [2] J. Thomson, et. al., "An Integrated 802.11a Baseband and MAC Processor," ISSCC Digest of Technical Papers, Paper 7.2, Feb. 2002.

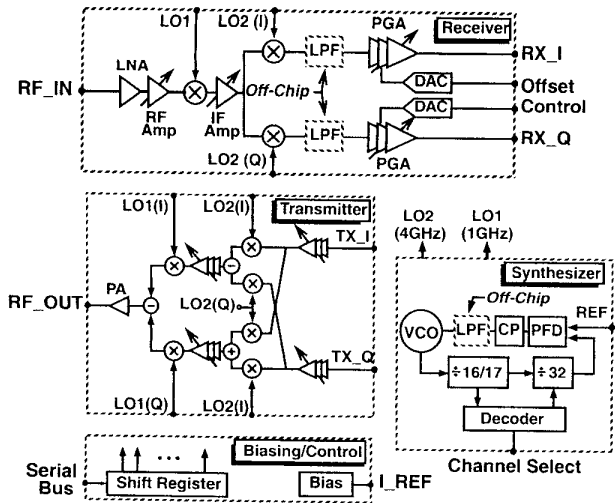


Figure 5.4.1: Block diagram of CMOS transceiver.

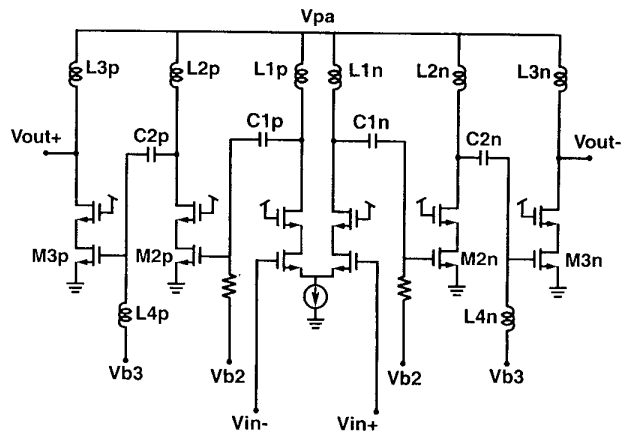


Figure 5.4.2: PA schematic.

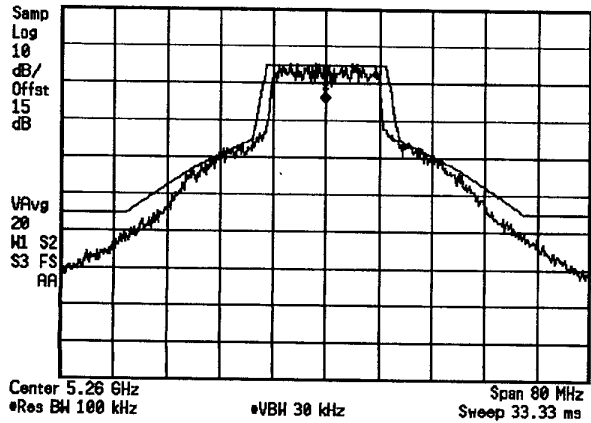


Figure 5.4.3: Measured 17dBm BPSK OFDM TX spectrum.

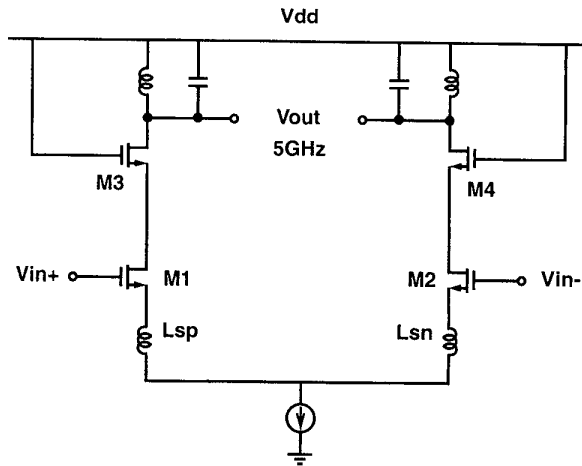


Figure 5.4.4: LNA schematic.

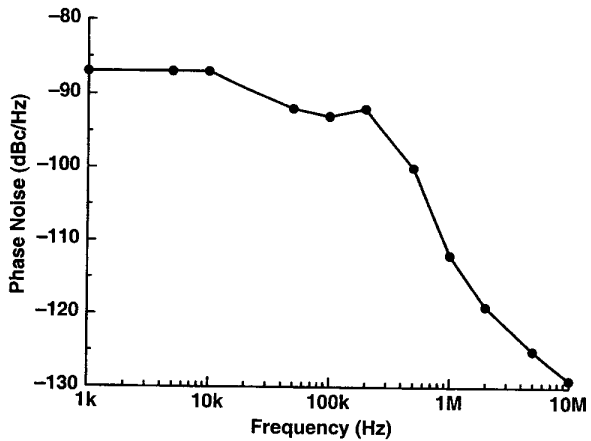


Figure 5.4.5: Measured synthesizer phase noise.

VDD	2.5V
VPA	3.3V
TX Chain Power Dissipation	64mA at 2.5V & 190mA at 3.3V
RX Chain Power Dissipation	100mA at 2.5V
Synthesizer Power Dissipation	72mA at 2.5V
TX Output Power Level	22dBm
Rx Chain Noise Figure	8dB
Rx Input P-1dB	-8.5dBm
Phase Noise (at 1MHz offset)	-112dBc/Hz
Technology	0.25 μ m 1P5M CMOS
Package	64-pin LPCC
Die Size	22mm ²

Figure 5.4.6: Measured performance summary.

Performance	Measured	Spec. Limit
RX sensitivity at 0.1% BER	-81.9dBm	≤ -70dBm
Max. sig. input at 0.1% BER	-19dBm	≥ -20dBm
CCI at 0.1% BER	10.9dB	≤ 14dB
± 1MHz ACI at 0.1% BER	0.5dB	≤ 4dB
± 2MHz ACI at 0.1% BER	-32.9dB	≤ -30dB
± 3MHz ACI at 0.1% BER	-43.8dB	≤ -40dB
Transmit output power	2.5dBm	<4 dBm >-6dBm
Modulation Characteristics	136kHz	≥ 115kHz
Transmit carrier offset	19kHz	≤ 75kHz
Transmit drift frequency	< ±11kHz	≤ ± 25kHz
Out of band emission	-59dBm	≤ -30dBm
TX ACP at ± 3MHz	<-42dBm	≤ -40dBm
DC current on RX at 3V	45mA	-
DC current on TX at 3 V	36mA	-
Operating temperature	-30° C to +85° C	-

Figure 5.3.7: Performance summary.

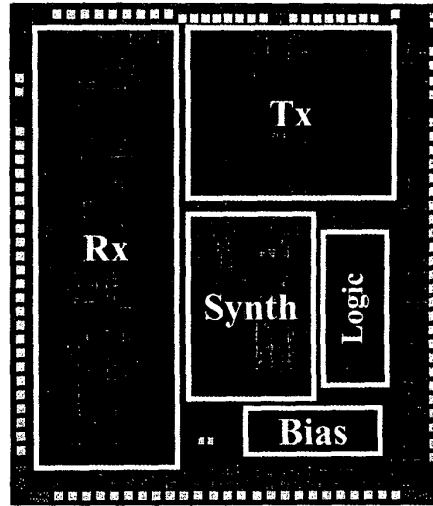


Figure 5.4.7: Die micrograph.

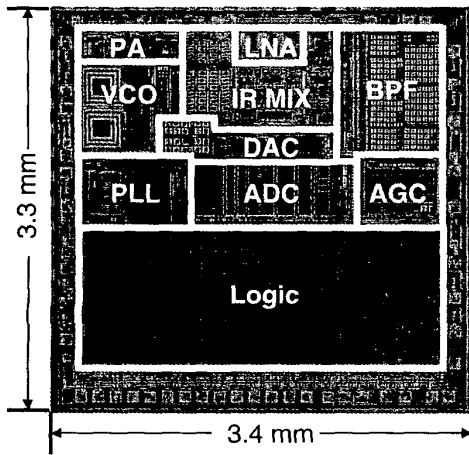


Figure 5.5.7: Chip micrograph.

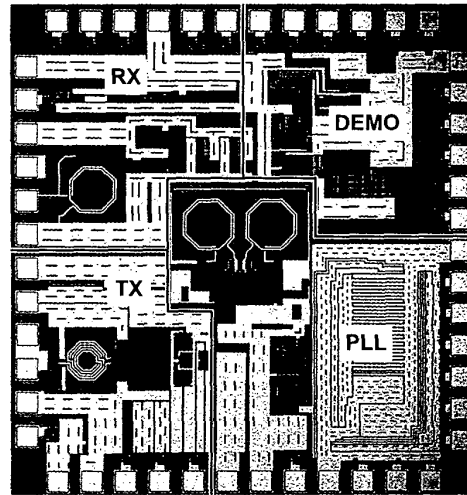


Figure 5.6.7: Micrograph of single-chip 5.8GHz ETC transceiver IC.

Table 6.2.1 Bank combination				
	Case I	Case II	Case III	Case IV
Code (Data) storage	8Mb	16Mb	24Mb	32Mb
Data (Code) storage	56Mb	48Mb	40Mb	32Mb

Bank 2				Bank 1
		Block R/D		
Data-line				
		Block R/D		
Bank 3		S/A		Bank 0

Figure 6.2.6: Chip micrograph.

Process	0.16µm CMOS triple metal
Cell size	0.27µm ²
Chip size	44.0mm ²
Organization	4M word / 8MB
Package	Stacked Multi-Chip Package with SRAM and PSRAM
Supply voltage	2.3V-3.6V
Access time	70ns(tACC/tCE)/25ns(tPAGE)

Figure 6.2.7: Key features.