

# On-Chip Interconnect Inductance – Friend or Foe (Invited)

S. Simon Wong, Patrick Yue, Richard Chang,  
So-Young Kim, Bendik Kleveland, Frank O'Mahony  
Center for Integrated Systems, Stanford University

## Abstract

*Inductance associated with on-chip wires can no longer be ignored as chip operation frequencies increase into GHz regime. Because the magnetic field propagates a very long range, the extraction of wire inductance is not just dependent on the immediate neighboring environment. This paper discusses the various difficulties of extracting inductance of randomly placed wires in a typical chip environment. With dedicated return path, the wire inductance can be controlled and benefit the design of high-speed circuits. Specific examples are illustrated.*

## 1. Introduction

As the operational frequencies of integrated circuits continue to increase beyond GHz, the inductive impedance associated with an on-chip wire will become comparable or dominant over the resistance component. This results in additional signal distortion, propagation delay, and cross-talk noise [1, 2]. Hence, it is necessary to extract the resistance  $R$ , capacitance  $C$  and inductance  $L$  of all the wires on a chip in order to accurately predict the performance and identify potential problems.

The extraction of  $R$  requires only the geometric information (width, height, length) and material properties (resistivity) of the wire. The extraction of  $C$  requires additional parameters (spacing and dielectric constant) of the immediate neighbor. Even in today's most complex chip, the extraction of  $R$  and  $C$  can be handled with the most advanced CAD tools.

## 2. Difficulties of Extracting $L$

$L$  describes the magnetic flux being generated by current flowing in a loop. Hence the return current path must be defined before  $L$  associated with a wire can be extracted. In a real chip environment in which the wires are randomly placed, the return path is ill defined and can be dynamic depending on the signal condition. Hence the extraction of  $L$  is significantly more difficult. In the partial element equivalent circuit approach, the self-inductance associated with each wire segment and the mutual inductance associated with each pair of wire segments are extracted and circuit simulation is then used to determine the return path and the  $L$  associated with each wire. Because of the long-range influence of magnetic field, the inductance matrix is usually very dense and not straightforward to sparsify. Simulation of this scale may not be practical.

In a typical chip, there is a large decoupling capacitance between ground and power, making them both effectively ac ground. A common assumption in extracting  $L$  is to restrict the current to return through the nearest ground or power line [3-6]. In a paper to be presented in this conference [7], we show that this assumption is only valid at very high frequencies when the return current seeks to minimize the loop inductance (and hence the size of the loop). At low frequencies, return current seeks to minimize the loop resistance instead. If there are multiple parallel ground or power wires (typically layout in a grid format), return currents can be widely spread to these parallel wires. Hence,  $L$  is the highest at low frequency and gradually decreases as frequency increases as shown in Figure 1.

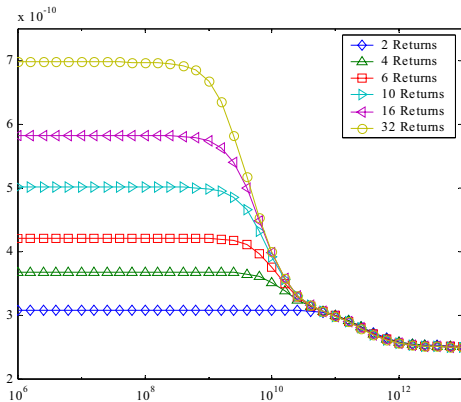


Fig. 1 –  $L$  versus frequency using different number of return paths.

In a real chip environment, in addition to the ground and power grids, there are random signal lines. The extraction of  $L$  under such an environment was examined in our previous work [8]. Two sets of test structures were implemented. A first set of ideal reference test structure is shown in top of Fig. 2. The interconnect process provides five layers of Al/Cu. The signal lines are in M5. Orthogonal ground lines are inserted in M4 in order to achieve a controlled capacitance. The signal line width and spacing  $S$  are varied over a wide range of values in order to observe the effect of coupling through the silicon substrate. A second set of realistic test structure as illustrated in the bottom of Fig. 2 has been designed to mimic as closely as possible a real chip including active drivers driving random lines, a regular power/ground grid in the topmost metal layers, and local power/ground routing at the lower metal layers. Details of the wiring network are described in [8].

The measured  $L$  versus line spacing  $S$  is shown in Fig. 3. Field solver simulation adequately predicts  $L$  of the reference test structure.  $L$  increases for increasing spacing because more flux is enclosed between the signal line and the return ground. In the realistic test structure,  $L$  becomes less dependent on the spacing to the intended return ground. The presence of random local lines and the capacitive coupling between them must have provided alternative return paths. In addition, there could be small local loops to support eddy currents resulting in opposing magnetic field and further reduction in  $L$ .

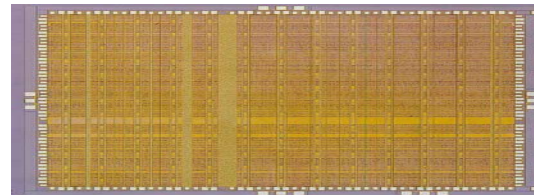
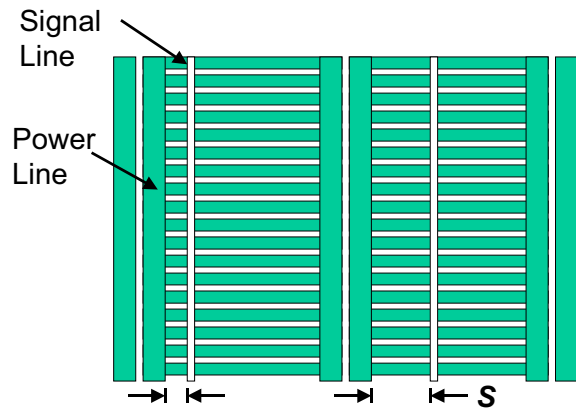


Fig. 2- Top is reference test structure. Bottom is micrograph of realistic test structure buried in a real chip environment.

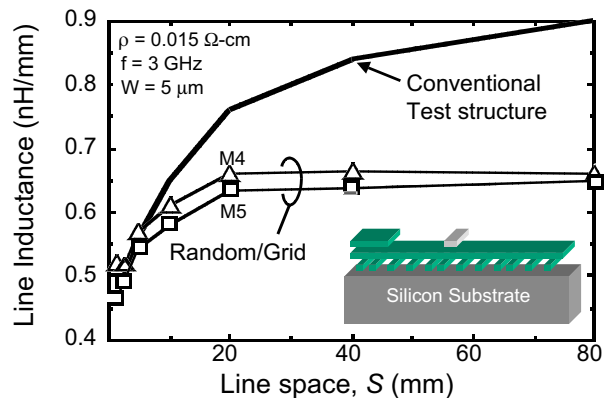


Figure 3 –  $L$  versus  $S$  for both test structures.

### 3. Taking Advantage of $L$

Although the extraction of  $L$  associated with a wire randomly placed in a chip is complicated by the factors described above.  $L$  can be controlled if there is a dedicated return path as in co-planar strip line, or micro-strip line (Fig. 4). Under such a controlled environment, the inductive behavior of the wire can actually provide a new design dimension as illustrated in the following examples.

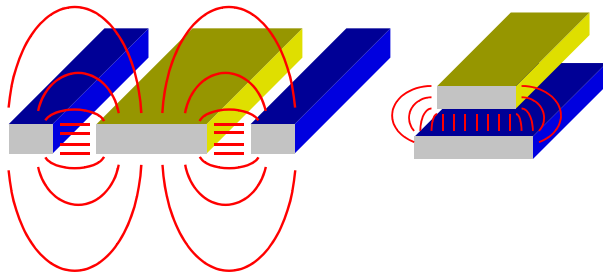


Fig. 4 – Left is co-planar strip line, right is micro-strip line.

#### A. Near Speed-of-Light Propagation of Electrical Signal

As a digital signal propagates down a long wire, the quality of the signal is degraded resulting in excessive delay or inter-symbol interference. To understand the reasons for this, the power spectral density of a 500 ps digital pulse is compared with the intrinsic frequency characteristics of a minimum-sized wire in Fig. 5. The digital signal is broadband in nature, while the wire characteristic changes dramatically over this frequency band. At lower frequencies, the wire behaves as a distributed  $R-C$  network. In this  $R-C$  regime, signals travel very slowly by diffusion and undergo frequency dispersion. As the frequency increases,  $L$  of the wire begins to dominate over  $R$ , and the wire behaves more as a  $L-C$  waveguide. The high-frequency  $L-C$  regime allows for propagation of an electromagnetic wave; consequently, the peak velocity is the speed-of-light in the dielectric surrounding the wire.

The characteristics shown in Fig. 5 suggest that a high-speed system can be built by taking advantage of the wave nature of wire [9]. At the same time, it is necessary to eliminate the low-frequency portion of the

signal that lags behind. This can be achieved by modulating the digital data with a sufficiently high-frequency carrier, and as a result, concentrating all of the signal power in the  $L-C$  regime. Furthermore, the crossover frequency between the  $R-C$  and  $L-C$  regimes must be lowered. By explicitly emphasizing  $L$  and reducing  $R$ , this transition can be shifted into the single GHz range. In this frequency range, simple RF circuits can be designed to transmit and receive these modulated signals. Figure 6 illustrates the impact of using modulated signaling in combination with an optimized low-loss wire to support high-speed transmission. The signal spectral components lie predominantly in this high-speed  $L-C$  region.

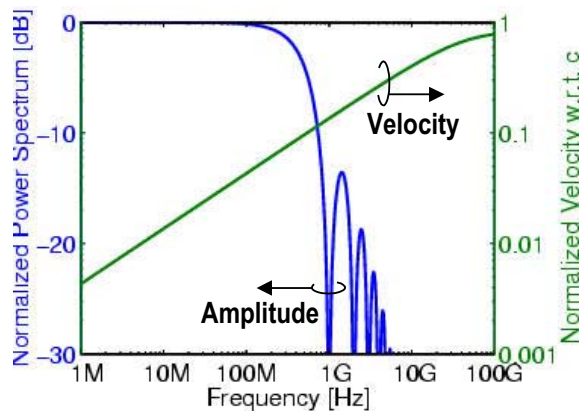


Fig 5 – Spectral power density of a typical digital pulse, and the signal propagation velocity versus frequency along a minimum-sized wire.

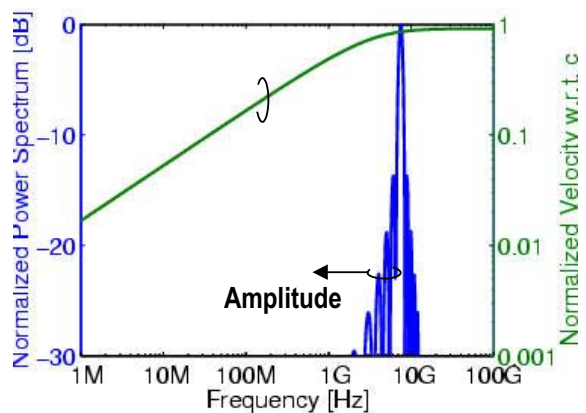


Figure 6 – Spectral power density of a modulated digital pulse, and the signal propagation characteristic of an optimized low-loss wire.

This system has been demonstrated in a TSMC 0.18- $\mu\text{m}$  standard logic CMOS technology with six levels of Al/Cu wiring and  $\text{SiO}_2$  dielectric. The differential carrier signals and digital input pulse are generated off-chip, while the transmitter, receiver, and all other components are integrated on-chip. Figure 7 shows sample as-measured input and output waveforms propagating over a distance of 2 cm. This includes a delay of 123 ps due to the inverters needed for driving signals on and off of the chip for testing and measurement. Subtracting the inverter delays yields an average delay of 283 ps, which corresponds to an effective signal propagation speed of nearly one-half the speed of light in  $\text{SiO}_2$ .

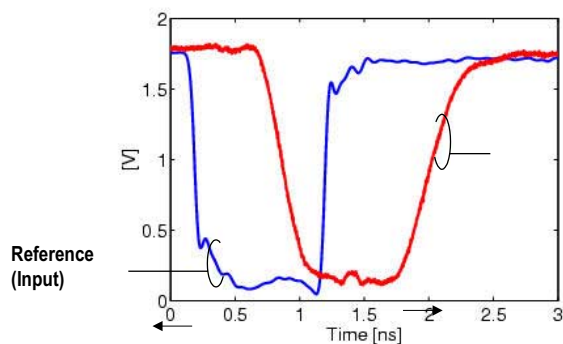


Fig. 7 – Measured input and output waveforms of the modulated signal transmission system.

## B. 10 GHz Standing Wave Clock

Global clock distribution has become increasingly difficult for multi-GHz microprocessors. Timing uncertainty must reduce with clock period, but skew and jitter for conventional H-trees are proportional to latency, which does not scale with clock period [10].

The global clock network in Fig. 8 distributes a 10 GHz clock through a grid of standing-wave oscillators (SWOs) [11]. The SWO, as shown in Fig. 9, is analogous to a differential L-C oscillator where the gain and tank are distributed. These SWOs are coupled together and sustain synchronous, sinusoidal standing waves across the chip. A single clock source coupled into one SWO injection-locks the entire grid. Clock buffers recover a digital clock and drive the local network.

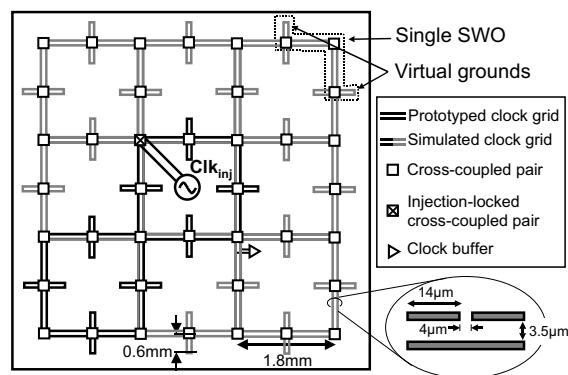


Fig. 8 – 10GHz global clock network with coupled standing wave oscillators.

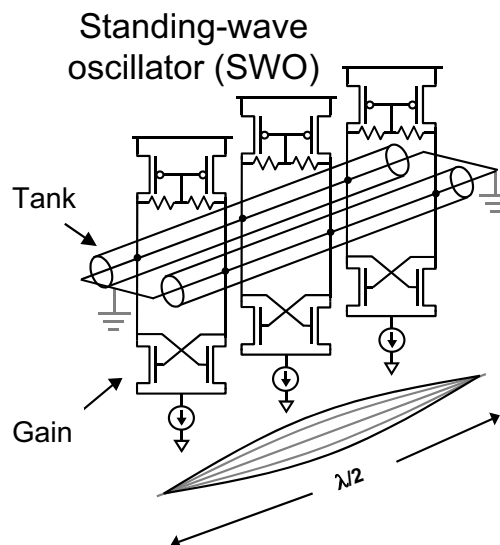


Fig. 9 – Schematic of a standing wave oscillator.

This coupled SWO clock network has been prototyped in a TSMC 0.18- $\mu\text{m}$  standard logic CMOS technology. The test chip integrates eight coupled SWOs. The grid injection locks to an external clock from 9.8 GHz to 10.5 GHz (6.4% locking range). The clock jitter measured through an open-drain buffer is 1.5 ps rms; however, the resolution of this measurement is limited by the 1.4 ps rms jitter of the signal generator used to lock the grid. Based on these values, the jitter added by the clock grid is estimated to be below 0.5 ps.

### C. 23GHz Bandwidth CMOS Distributed Amplifier

In a state-of-the-art CMOS technology, the parasitic I/O capacitance, including the electrostatic discharge protection circuitry, is typically in the range of 2-8 pF. At high frequencies, the reactance associated with this large capacitance becomes comparable to the 50-Ω characteristic impedance of the package and board interfaces. The impedance mismatch due to the parasitic capacitance causes significant reflection and severely limits the inter-chip signal bandwidth.

The bandwidth limitation due to the large parasitic capacitance can be overcome by using the principle of distributed amplification. An artificial transmission line that matches the target characteristic impedance can be implemented by combining the parasitic capacitance with low-loss inductors [12] or *L-C* lines [13]. A five-segment distributed amplifier with *L-C* lines is illustrated in Fig. 10. The transistor is divided into five equal segments with the gate inputs and drain outputs connected with *L-C* lines. The amplifier effective input capacitance is hence reduced to one fifth that of the total transistor. The measured S-parameters are shown in Fig. 11. The input impedance match is excellent as expected. The return loss ( $S_{11}$ ) is as low as -14 dB from dc to 18 GHz. The unity gain bandwidth is 23 GHz after input/output pad extraction.

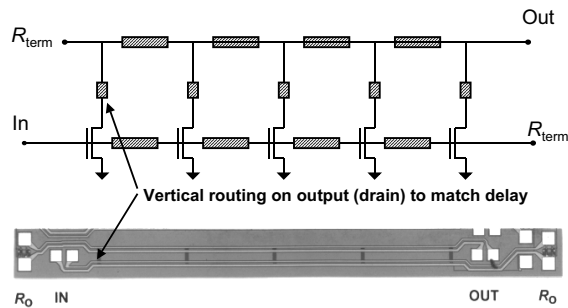


Fig. 10 – Schematic and micrograph of a distributed amplifier.

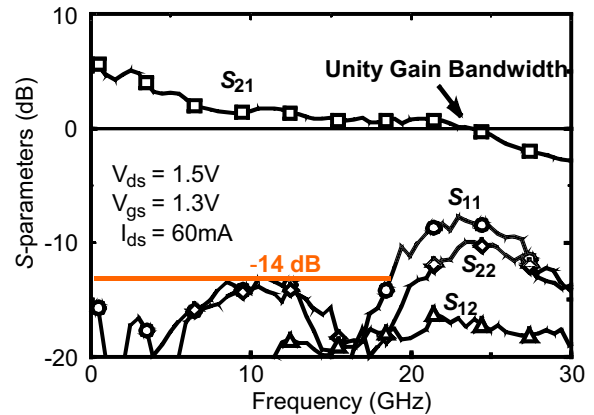


Fig. 11 – Measured performance of the distributed amplifier.

### D. 16GHz CMOS Distributed Oscillator

A distributed oscillator is realized by connecting the output of a distributed amplifier back to the input, as illustrated in Fig. 12 [13]. The oscillation that builds up experiences the *L-C* line delay plus the average of one gate delay around the loop. The measured operating frequency is 16.6 GHz.

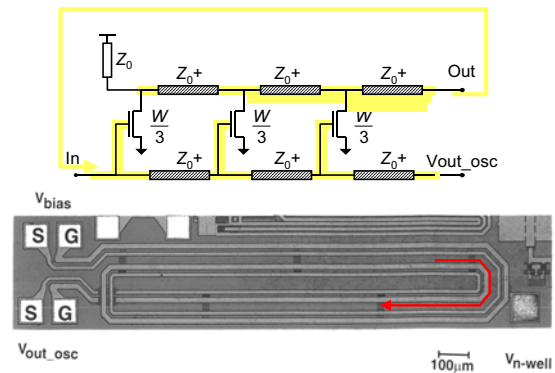


Fig. 12 – Schematic and micrograph of a distributed oscillator.

#### 4. Conclusions

In high frequency operations, wire inductance can no longer be ignored. The extraction of wire inductance in a typical chip is complicated by the poorly defined current return path and the influence of the surrounding wiring network. In a controlled environment with dedicated return path, the wire inductance is well defined. The inductor behavior can be exploited for novel design concepts. Demonstration examples include near speed-of-light propagation of electrical signal, 10GHz standing wave clock distribution, 23 GHz distributed amplifier and 16 GHz distributed oscillator.

#### 5. References

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