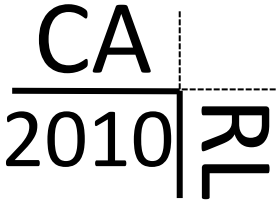
Workshop on the Intersections of Computer Architecture and Reconfigurable Logic
(CARL 2010)
Atlanta, Georgia - Sunday, December 5, 2010
Co-located with MICRO-43
http://www.ece.cmu.edu/calcm/carl2010

Technical Program Committee

- Dave Albonesi, Cornell University
- Derek Chiou, UT Austin
- John Davis, Microsoft Research
- Srini Devadas, MIT
- Joel Emer, Intel/MIT
- James Hoe, CMU
- Shih-Lien Lu, Intel
- Robert Mullins, University of Cambridge
- David Penry, Brigham Young University
- Sunil Shukla, IBM
- Satnam Singh, Microsoft Research
- Chuck Thacker, Microsoft Research
- Kees Vissers, Xilinx
- Hong Wang, Intel
- John Wawrzynek, UC Berkeley

Organizers

- Derek Chiou, UT Austin
- Joel Emer, Intel/MIT
- James C. Hoe, CMU



The Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL) is a new forum for presenting FPGA and reconfigurable logic research relevant to a computer architecture audience. In recent years, there has been a renewed interest in reconfigurable computing, driven by the need for greater computing performance and, at the same time, better power and energy efficiency. Reconfigurable computing is a key technology candidate to efficiently leverage exponential device scaling beyond current multicore processors. This full-day workshop will be held on Sunday, December 5, 2010, co-located with MICRO-43 in Atlanta, Georgia. The meeting will include keynote presentations, research presentations and a brainstorming panel discussion.

We invite research papers from all areas of FPGA and reconfigurable logic that impact the computer architecture community. Major areas of interests include, but are not limited to:

- New FPGA architectures and reconfigurable fabric designed to support computing
- Heterogeneous computing processors and systems that incorporate reconfigurable logic
- Computation models and programming tools for reconfigurable and heterogeneous computing
- State-of-the-art (ready-for-use) reconfigurable computing platforms and infrastructure
- Algorithms and applications for reconfigurable computing (including FPGA-based prototyping and simulation of computer systems)
- Evaluations of reconfigurable computing in terms of performance, power/energy, flexibility and cost, especially in comparison to other hardware paradigms (multicore, GPU, ASICs, etc.).

We will accept submissions in two categories: (1) new unpublished manuscripts, and (2) audience-appropriate revisions of papers already published or under review outside of traditional computer architecture forums. Accepted papers will be disseminated informally on the workshop's website.

A submission should be 4~6 pages in double-column format. The review process is not blind; please include authors' names and affiliations. Please clearly indicate whether a submission is category 1 or 2. If category 2, the source materials must be clearly identified in the abstract and introduction.

Please visit the conference website (http://www.ece.cmu.edu/calcm/carl2010) for submission. Please email questions to jhoe@ece.cmu.edu.

Important Dates

Submission Deadline: October 1, 2010
Notification of Selection: November 1, 2010
Final Paper Submission: November 15, 2010