are summarized below. Table I gives the key architectural characteristics of the multicore system. All five systems run at $105.5MHz$, which is the clock frequency of the router, regardless of the size of the mesh.

Core	
ISA	32-Bit MIPS
Hardware threads	1
Pipeline Stages	7
Bypassing	Full
Branch policy	Always non-Taken
Outstanding memory requests	1
Level 1 Instruction/Data Caches	
Associativity	Direct
Size	variable
Outstanding Misses	1
On-Chip Network	
Topology	2D-Mesh
Routing Policy	DOR and Table-based
Virtual Channels	2
Buffers per channel	8

TABLE I
2D-MESH SYSTEM ARCHITECTURE DETAILS.

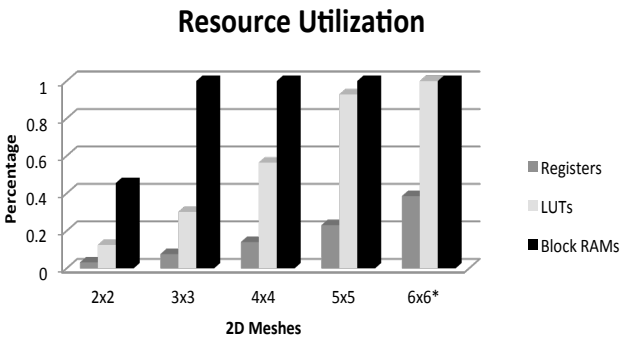

Fig. 10. Percentage of FPGA resource utilization per mesh size.

Figure 10 summarizes the FPGA resource utilization by the different systems in terms of registers, lookup tables, and block RAMs. In the 2×2 and 3×3 configurations, the local memory is set to $260KB$ per core. The 3×3 configuration uses 99% of block RAM resources at $260KB$ of local memory per core. For the 4×4 configuration the local memory is reduced to $64KB$ per core, and the local memory in the 5×5 configuration is set to $32KB$. The 6×6 configuration, with $16KB$ of local memory per core, fails during map and router, due to lack of LUTs.

IV. Conclusion

In this work, we present the new *Heracles* design toolkit which is comprised of the soft hardware (HDL) modules, application compiler, and a graphical user interface. It is a component-based framework that gives researchers the ability to create complete, realistic, synthesizable, multi/many-core architecture for fast and high accuracy design space exploration. In this environment, user can explore design trade-offs at the processing unit level, the memory organization and access level, and the network on-chip level. The *Heracles* tool is open-source and can be downloaded at http://projects.csail.mit.edu/heracles/.

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