

are summarized below. Table I gives the key architectural characteristics of the multicore system. All five systems run at 105.5MHz , which is the clock frequency of the router, regardless of the size of the mesh.

Core	
ISA	32-Bit MIPS
Hardware threads	1
Pipeline Stages	7
Bypassing	Full
Branch policy	Always non-Taken
Outstanding memory requests	1
Level 1 Instruction/Data Caches	
Associativity	Direct
Size	variable
Outstanding Misses	1
On-Chip Network	
Topology	2D-Mesh
Routing Policy	DOR and Table-based
Virtual Channels	2
Buffers per channel	8

TABLE I
2D-MESH SYSTEM ARCHITECTURE DETAILS.

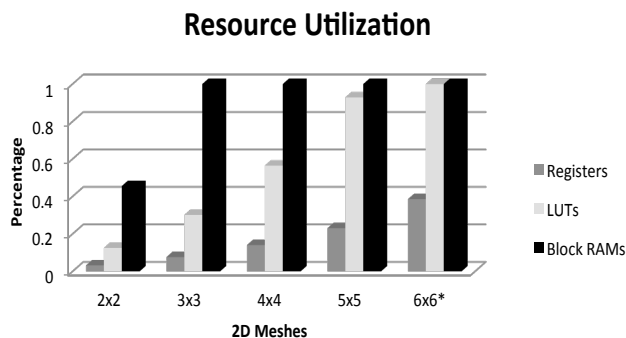


Fig. 10. Percentage of FPGA resource utilization per mesh size.

Figure 10 summarizes the FPGA resource utilization by the different systems in terms of registers, lookup tables, and block RAMs. In the 2×2 and 3×3 configurations, the local memory is set to 260KB per core. The 3×3 configuration uses 99% of block RAM resources at 260KB of local memory per core. For the 4×4 configuration the local memory is reduced to 64KB per core, and the local memory in the 5×5 configuration is set to 32KB . The 6×6 configuration, with 16KB of local memory per core, fails during map and router, due to lack of LUTs.

IV. CONCLUSION

In this work, we present the new *Heracles* design toolkit which is comprised of the soft hardware (HDL) modules, application compiler, and a graphical user interface. It is a component-based framework that gives researchers the ability to create complete, realistic, synthesizable, multi/many-core architecture for fast and high accuracy design space exploration. In this environment, user can explore design trade-offs at the processing unit level, the memory organization and access level, and the network on-chip level.

The *Heracles* tool is open-source and can be downloaded at <http://projects.csail.mit.edu/heracles/>.

REFERENCES

- [1] M. Kinsy, M. Pellauer, and S. Devadas, "Heracles: Fully synthesizable parameterized MIPS-based multicore system," in *Field Programmable Logic and Applications (FPL), 2011 International Conference on*, sept. 2011, pp. 356–362.
- [2] P. S. Magnusson, M. Christensson, J. Eskilson, D. Forsgren, G. Hällberg, J. Högberg, F. Larsson, A. Moestedt, and B. Werner, "Simics: A full system simulation platform," *Computer*, vol. 35, no. 2, pp. 50–58, Feb. 2002.
- [3] W. Yu, "Gems a high performance em simulation tool," in *Electrical Design of Advanced Packaging Systems Symposium, 2009. (EDAPS 2009). IEEE*, dec. 2009, pp. 1–4.
- [4] M. Lis, P. Ren, M. H. Cho, K. S. Shim, C. Fletcher, O. Khan, and S. Devadas, "Scalable, accurate multicore simulation in the 1000-core era," in *Performance Analysis of Systems and Software (ISPASS), 2011 IEEE International Symposium on*, april 2011, pp. 175–185.
- [5] J. Miller, H. Kasture, G. Kurian, C. Gruenwald, N. Beckmann, C. Celio, J. Eastep, and A. Agarwal, "Graphite: A distributed parallel simulator for multicores," in *High Performance Computer Architecture (HPCA), 2010 IEEE 16th International Symposium on*, jan. 2010, pp. 1–12.
- [6] M. Pellauer, M. Adler, M. Kinsy, A. Parashar, and J. Emer, "Hasim: FPGA-based high-detail multicore simulation using time-division multiplexing," in *High Performance Computer Architecture (HPCA), 2011 IEEE 17th International Symposium on*, feb. 2011, pp. 406–417.
- [7] Z. Tan, A. Waterman, R. Avizienis, Y. Lee, H. Cook, D. Patterson, and K. Asanovic and, "Ramp gold: An FPGA-based architecture simulator for multiprocessors," in *Design Automation Conference (DAC), 2010 47th ACM/IEEE*, june 2010, pp. 463–468.
- [8] K. E. Fleming, M. Adler, M. Pellauer, A. Parashar, A. Mithal, and J. Emer, "Leveraging latency-insensitivity to ease multiple FPGA design," in *Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays*, ser. FPGA '12. New York, NY, USA: ACM, 2012, pp. 175–184.
- [9] P. Del valle, D. Atienza, I. Magan, J. Flores, E. Perez, J. Mendias, L. Benini, and G. Micheli, "A complete multi-processor system-on-chip FPGA-based emulation framework," in *Very Large Scale Integration, 2006 IFIP International Conference on*, oct. 2006, pp. 140–145.
- [10] J. Andersson, J. Gaisler, and R. Weigand. Next generation multipurpose microprocessor. Available at: <http://microelectronics.esa.int/ngmp/NGMP-DASIA10-Paper.pdf>.
- [11] C. R. Clack, R. Nathuji, and H.-H. S. Lee. Using an FPGA as a prototyping platform for multi-core processor applications. In *Workshop on Architecture Research using FPGA Platforms*, Cambridge, MA, 2005.
- [12] A. Lusala, P. Manet, B. Rousseau, and J.-D. Legat, "Noc implementation in FPGA using torus topology," in *Field Programmable Logic and Applications, 2007. FPL 2007. International Conference on*, aug. 2007, pp. 778–781.
- [13] N. Genko, D. Atienza, G. De Micheli, J. Mendias, R. Hermida, and F. Catthoor, "A complete network-on-chip emulation framework," in *Design, Automation and Test in Europe, 2005. Proceedings*, march 2005, pp. 246–251 Vol. 1.
- [14] N. Banerjee, P. Vellanki, and K. Chatha, "A power and performance model for network-on-chip architectures," in *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, vol. 2, feb. 2004, pp. 1250–1255 Vol.2.
- [15] N. Saint-Jean, G. Sassatelli, P. Benoit, L. Torres, and M. Robert, "Hs-scale: a hardware-software scalable mp-soc architecture for embedded systems," in *VLSI, 2007. ISVLSI '07. IEEE Computer Society Annual Symposium on*, march 2007, pp. 21–28.
- [16] D. Patterson and J. Hennessy, *Computer Organization and Design: The Hardware/software Interface*. Morgan Kaufmann, 2005.
- [17] M. H. Cho, K. S. Shim, M. Lis, O. Khan, and S. Devadas, "Deadlock-free fine-grained thread migration," in *Networks on Chip (NoCS), 2011 Fifth IEEE/ACM International Symposium on*, may 2011, pp. 33–40.
- [18] W. J. Dally and B. Towles, *Principles and Practices of Interconnection Networks*. Morgan Kaufmann, 2003.
- [19] L. M. Ni and P. K. McKinley, "A survey of wormhole routing techniques in direct networks," *Computer*, vol. 26, no. 2, pp. 62–76, 1993.