TRAINING IP CREATORS AND INTEGRATORS

Don Bouldin, Senthil Natarajan, Benjamin Levine, Chandra Tan and Danny Newport

Electrical Engineering
University of Tennessee
Knoxville, TN 37996-2100
dbouldin@utk.edu

ABSTRACT

Intellectual property (IP) blocks are being created for reuse and marketed as a means of reducing the development time of complex designs. This in turn leads to a reduction in time to market which results in increased profits. Alliances of companies have been formed to support an open market for IP and standards are being devised to ensure the quality of this IP. Also, a web-based network has been set up to facilitate the matching of providers and consumers. However, a significant problem still needs be addressed: namely, the widespread training of IP creators and integrators. In recent years, universities have been offering courses which involve logic synthesis and simulation using VHDL or Verilog along with verification using FPGAs. Now that standards for IP reuse are being developed, these courses need to require students to develop and integrate IP blocks which are compliant with the desired quality level. In this paper, we describe the procedure that we have begun using at the University of Tennessee to train IP creators and integrators to meet these new challenges. In addition, we propose the widespread adoption of this type of training and the development of an infrastructure to support the dissemination of IP shareware.

1. INTRODUCTION

During the 1990's, universities have been offering courses which involve logic synthesis using VHDL or Verilog along with verification using field-programmable gate arrays (FPGAs). However, with the emergence of standards for IP reuse, these courses need to require students to develop and integrate IP blocks which are compliant with the desired quality level.

At the University of Tennessee, we have adopted a procedure to train students to create and integrate IP that is reusable. This procedure exploits the use of reconfigurable logic since FPGA-based platforms provide a significant decrease in design time of digital applications over conventional means. Such a decrease can only serve to benefit the designers of an application by providing them with more time for thorough system-level testing and/or less time-to-market for a given application. The nature of the savings in time by using IPs within an FPGA-based technology is two-fold. First, the inherent nature of reconfigurable logic makes it quick to implement a design without the delays associated with fabricating prototypes for system-level testing. Second, the use of pre-validated, pre-verified, and pre-characterized hardware IP blocks that are reusable can similarly serve to quicken an application's design time. This is due primarily to the fact that IP blocks will already have been tested adequately enough to ensure proper functionality. This allows a digital design team the flexibility of working on a higher level of abstraction since they no longer have to get involved with how the individual IP blocks work. So long as an IP block meets timing, area, power, and functionality requirements, designers can reuse these blocks to make more efficient use of their time. Therefore, adequate testing is pivotal for hardware IP blocks to have much practical use.

2. IP CREATION

To be reusable, an IP block must behave identically when used alone or in conjunction with other blocks. The first step towards achieving this goal is defining precisely a block's parameters and its explicit functionality. Such specifications serve as a model which will later be used to compare to the behavior of a hardware-equivalent representation. Since this model will most likely be described using words and equations rather than source code, few test cases should be applied to this model. A more exhaustive set of test cases should be reserved for computer-aided simulations and hardware verification.

Computer-aided simulations ensure the validity of an IP model. The highest level simulation can be a software (C, Matlab, Khoros, etc) version of the IP model. This software version serves to both ensure the validity of the theoretical IP model and generate output vectors for a set of applied input test vectors. These input and output vectors together constitute a test bench that can be used on the remaining computer simulations and during the hardware verification stage.

Evaluating the software implementation may force the need to modify the original IP model. However, once a software prototype is finished, a hardware description language such as VHDL or Verilog can be used to model a hardware version of the IP model. Using CAD tools, this code can be synthesized to generate a digital circuit, which can then be targeted for a specific technology using place and route CAD software. The synthesized circuit is simulated with the previously generated test bench to ensure the validity of the hardware model. A post-layout simulation of the final circuit on the target technology serves as the third and final test for the hardware IP validity. At this stage, the hardware design is ready for execution on an FPGA platform. Verification of the hardware execution entails applying the same test bench to the hardware and observing its outputs. The hardware model passes this verification stage when its results concur with those of the three computer-aided simulations. Once verified, the hardware IP can be completely characterized in terms of size, delay, power consumption, and functionality. After being validated, verified, and char-

acterized, the hardware IP block is now ready for use in larger applications.

3. IP ACQUISITION

In addition to IP creation, students need to be trained to perform IP integration. The first step in this process involves the acquisition of previously developed and tested IP. Presently, almost all IP blocks of interest are too expensive to be afforded by a single university for use in courses. Therefore, we propose two solutions: consortium and shareware.

A consortium of interested universities might be formed to aggregate funds (or equivalent buying power) to acquire previously created IP from vendors. The consortium would negotiate with a vendor for one master copy of the IP and then distribute that IP among its members. Thus, the consortium appears to the vendor as one large customer rather than as numerous, and perhaps poor and annoying, small customers. The drain on the vendor would be less so the price to the consortium would likely be significantly less than what a single university would normally be required to pay.

In parallel with the organizing of one or more consortia, universities might wish to develop a shareware system in which IP blocks created at one university would be contributed to a central database and disseminated freely to others. The blocks need not be direct competition for commercially-available blocks but instead might be simpler versions that would be sufficient for training but inadequate for commercial products.

4. IP INTEGRATION

With the availability of IP blocks, students could then gain experience with IP integration. This process will likely involve the use of a design team with several students working together to produce a significant system. Employers frequently cite their desire that students gain such teaming experience while in school since designers generally work in teams on the job.

One means of enabling students to gain experience with IP integration and working as a team is to use reconfigurable logic platforms such as the Wildforce board offered by Annapolis Microsystems, Inc. This board is a standard size PCI card containing four large Xilinx FPGAs or processing elements (PEs). The PEs can be as small as 13,000-gate parts or as large as 62,000-gate parts, giving a system gate count between 52,000 and 333,000 gates. Hence, systems of significant size can be developed and verified in the laboratory.

5. CONCLUSIONS

The training of students in universities (and for that matter, those already in industry) needs to involve IP creation and integration that is compliant with emerging standards. A procedure for IP creation which is presently being utilized in a course has been described. Proposals for the acquisition and sharing IP to facilitate IP integration were also presented. These proposals have been put forward for discussion and possible widespread adoption within the university and design communities.