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BENJAMIN A. LEVINE, PH.D.

OBJECTIVE

To obtain a challenging position researching, designing, and implementing advanced computer hardware, programmable logic, or other digital systems.

EDUCATION

- **Ph.D., Electrical and Computer Engineering, Carnegie Mellon University,** Pittsburgh, PA.
  Graduated May 2005. Advisor: Dr. Herman H. Schmit.
  Thesis: *HASTE: Hybrid Architectures with a Single, Transformable Executable.*
- **M.S., Electrical Engineering, University of Tennessee**, Knoxville, TN.
  Graduated May 1999. Advisor: Dr. Donald W. Bouldin.
  Thesis: *A System for the Implementation of Image Processing Algorithms on Configurable Computing Hardware.*
- **B.S., Electrical Engineering, University of Tennessee**, Knoxville, TN.
  Graduated May 1997. Minor in Mathematics.

RELEVANT PROFESSIONAL EXPERIENCE

- November 2004 – Present Carnegie Mellon University Pittsburgh, PA
  Researcher & Instructor: Currently investigating the use of Content Addressable Memory for accelerating automatic target recognition applications. Project is joint research between CMU, Northrop Grumman, and the University of Pittsburgh, sponsored by the Dept. of Defense. Taught senior digital hardware design class.
- September 2003 – August 2004 University of Pittsburgh Pittsburgh, PA
  Assistant Professor, Department of Electrical Engineering: Performed research in computer architecture and digital systems, particularly reconfigurable computing and programmable logic. Supervised graduate student research. Taught computer architecture classes.
- August 1999 – August 2003 Carnegie Mellon University Pittsburgh, PA
  Graduate Research Assistant, IBM/SRC Graduate Fellow: Developed tools for evaluation of reconfigurable fabrics and application mapping to such fabrics. Investigated hardware requirements for, and performance of, diverse benchmark applications on these fabrics. Assisted in technology transfer of PipeRench technology from CMU to industrial licensees. Involved in the design, verification, and testing of the CMU PipeRench reconfigurable computing architecture, a 3.6 million transistor, six metal layer, 0.18 micron IC. Implemented a demonstration system using PipeRench to decrypt video streams in real-time. Implemented major hardware design changes in PipeRench and related changes needed in software tools, including the compilation flow and the verification suite. Investigated implementation of advanced error-correction codes using FPGA-based hardware.
- May 2000 – August 2000 Northrop Grumman Electronic Systems Pittsburgh, PA
  April 2002 – September 2002
  Research Intern/Engineer: Investigated implementation of target recognition algorithms using PipeRench. Evaluated power consumption and performance compared to competing technologies and determined architectural changes needed to enable improved performance. Implemented applications using prototype PipeRench chips and FPGA based hardware. Implemented both hardware and software for prototype PipeRench system.
- May 1998 – May 1999 University of Tennessee Knoxville, TN
  Graduate Research Assistant: Worked on the CHAMPION project, part of the DARPA ACS program. Helped develop a system for the automatic implementation of image processing algorithms expressed in Khoros Cantata, a graphical programming environment, on FPGA-based reconfigurable computing hardware.

PUBLICATIONS, PRESENTATIONS, & PATENTS

- "Implementation of Target Recognition Applications Using Pipelined Reconfigurable Hardware," presented at the Military and Aerospace Programmable Logic Devices International Conference, September 2003.
- "Application Representation for HASTE: Hybrid Architectures with a Single Transformable Executable," in *Proc. IEEE Symposium on Field-Programmable Custom Computing Machines,* 2003, pp 101-110 (With H. Schmit).
- "Hardware Compilation in Hardware: Enabling Integration of Reconfigurable Fabrics and Processors," presented at the SRC GFP Conference, Dallas, TX, September 2002 (presentation only).
- "PipeRench: Power & Performance Evaluation of a Programmable Pipelined Datapath," presented at Hot Chips 14, Palo Alto, CA, August 2002 (presentation only, with H. Schmit).
- "PipeRench: A Virtualized Programmable Datapath in 0.18 Micron Technology," in *Proc. IEEE Custom Integrated Circuits Conference,* 2002, pp. 63-66 (with H. Schmit, D. Whelihan, A. Tsai, M. Moe, R. Taylor).
- "Queue Machines: Hardware Compilation in Hardware," in *Proc. IEEE Symposium on Field-Programmable Custom Computing Machines,* 2002, pp. 152-160 (with H. Schmit, B. Ylvisaker).
- "Implementation of Near Shannon Limit Error-Correction Codes Using Reconfigurable Hardware," in *Proc. IEEE Symposium on Field-Programmable Custom Computing Machines,* 2000, pp. 217-226 (with R. Taylor, H. Schmit).
- "Automatic Mapping of Khoros-based Applications to Adaptive Computing Systems," in *Proc. Military and Aerospace Applications of Programmable Devices and Technologies International Conference*, 1999, pp. 101-107 (with S. Natarajan, C. Tan, D. Newport, D. Bouldin).
- "Training IP Creators and Integrators," in *Proc. IEEE International Conference on Microelectronic Systems Education*, 1999, pp. 4-5 (with D. Bouldin, S. Natarajan, C. Tan, D. Newport).
- "Mapping of an Automated Target Recognition Application from a Graphical Software Environment to FPGA-based Reconfigurable Hardware," in *Proc. IEEE Symposium on Field-programmable Custom Computing Machines,* 1999, pp. 292-293 (with S. Natarajan, C. Tan, D. Newport, D. Bouldin).

U.S. Patents: One pending, Application #20040034804: "Programmable pipeline fabric having mechanism to terminate signal propagation"

AWARDS AND HONORS RECEIVED

IBM/SRC Graduate Research Fellowship
University of Tennessee College of Engineering Haensler Scholarship
Phi Kappa Phi Honor Society
Tau Beta Pi Engineering Honor Society
Eta Kappa Nu Electrical and Computer Engineering Honor Society

REFERENCES:

Available on request.