

# Brian T. Gold

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## Education

Ph.D. Computer Engineering, Carnegie Mellon University, *expected* May 2009.

*Dissertation:* Increasing Processor Dependability in Distributed Shared-Memory Servers.

*Committee:* Babak Falsafi (advisor), James C. Hoe, Ken Mai, and Nhon Quach (Microsoft).

M.S. Computer Engineering, Virginia Tech, 2003.

*Thesis:* Balancing Performance, Area, and Power in an On-Chip Network.

B.S. Electrical Engineering, B.S. Applied Mathematics, Virginia Tech, 2001.

*Honors:* *Summa Cum Laude* (GPA: 3.98/4.0), Phi Beta Kappa, Tau Beta Pi.

## Academic Honors

### IEEE Micro ‘Top Picks’, 2004

Our paper, “Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth,” was selected as one of the top publications in computer architecture conferences for 2004.

### National Defense Science & Engineering Graduate (NDSEG) Fellowship

One of 200 students awarded this three-year fellowship from the DoD. Sponsored by the High-Performance Computing Modernization Program. 8/2004 to 5/2007.

### National Science Foundation (NSF) Graduate Research Fellowship

One of 900 students awarded this three-year fellowship from the NSF. 8/2001 to 5/2003.

### Northrop Grumman Graduate Fellowship

Award given by Northrop Grumman to two students in ECE at CMU. 8/2003 to 5/2004.

### Computer Architecture Lab at Carnegie Mellon (CALCM) Graduate Fellowship

Fellowship for graduate students in Computer Architecture at CMU. 8/2003 to 5/2004.

### Harry Lynde Bradley Scholarship

Three-year full scholarship to Virginia Tech, awarded by the ECE department. 8/1998 to 5/2001.

## Selected Publications

**Brian T. Gold**, Babak Falsafi, James C. Hoe, and Ken Mai. “Redac: Distributed, Asynchronous Redundancy in Shared-Memory Servers.” In Submission, Nov. 2008. Also available as *Computer Architecture Lab at Carnegie Mellon (CALCM) Technical Report 2008-002*.

David Meisner, **Brian T. Gold**, and Thomas F. Wenisch. “PowerNap: Eliminating Server Idle Power.” In *ACM/IEEE Int’l Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS ’09)*, Mar. 2009.

**Brian T. Gold**, Michael Ferdman, Babak Falsafi, and Ken Mai. “Mitigating Multi-bit Soft Errors in L1 Caches Using Last Store Prediction.” In *Workshop on Architectural Support for Gigascale Integration (ASGI-07)*, June 2007.

Jared C. Smolens, **Brian T. Gold**, James C. Hoe, Babak Falsafi, and Ken Mai. “Detecting Emerging Wearout Faults.” In *Workshop on Silicon Errors in Logic - System Effects (SELSE-3)*, Apr. 2007.

Jared C. Smolens, **Brian T. Gold**, Babak Falsafi, and James C. Hoe. “Reunion: Complexity-Effective Multicore Redundancy.” In *ACM/IEEE Int’l Symp. on Microarchitecture (MICRO-39)*, Dec. 2006.

**Brian T. Gold**, Jared C. Smolens, Babak Falsafi, and James C. Hoe. “The Granularity of Soft-Error Containment in Shared-Memory Multiprocessors.” In *Workshop on System Effects of Logic Soft Errors (SELSE-2)*, Apr. 2006.

**Brian T. Gold**, Jangwoo Kim, Jared C. Smolens, Eric S. Chung, Vasileios Liaskovitis, Eriko Nurvitadhi, Babak Falsafi, James C. Hoe, and Andreas G. Nowatzky. “TRUSS: A Reliable, Scalable Server Architecture.” In *IEEE Micro Special Issue on Reliability-Aware Microarchitectures*, Nov-Dec 2005.

**Brian T. Gold**, Anastassia Ailamaki, Larry Huston, and Babak Falsafi. “Accelerating Database Operators Using a Network Processor.” In *1st Int’l Workshop on Data Management on New Hardware (DaMoN)*, June 2005.

Jared C. Smolens, **Brian T. Gold**, Jangwoo Kim, Babak Falsafi, James C. Hoe, and Andreas G. Nowatzky. “Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth.” In *ACM/IEEE Int’l Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS XI)*, Oct. 2004.

Also in *IEEE Micro’s ‘Top Picks’ from 2004*.

James M. Baker, **Brian T. Gold**, Mark Bucciero, Sidney Bennett, Rajneesh Mahajan, Priyadarshini Ramachandran, and Jignesh Shah. “SCMP: A Single-Chip Message-Passing Parallel Computer.” In *Journal of Supercomputing*, 30(2): pp. 133-149, Nov. 2004.

## Patents

“System and method for efficiently visualizing and comparing communication network system performance.” Theodore S. Rappaport, Roger R. Skidmore, and **Brian T. Gold**. U.S. Serial No. 7,286,971. October 23, 2007.

“System, method, and apparatus for portable design, deployment, test, and optimization of a communication network.” Theodore S. Rappaport, **Brian T. Gold**, and Roger R. Skidmore. U.S. Serial No. 6,971,063. November 29, 2005.

## Teaching Experience

Teaching Assistant, Multiprocessor Computer Architecture, Spring 2005. (Babak Falsafi).

Teaching Assistant, Multiprocessor Computer Architecture, Spring 2004. (Andreas Nowatzky).

## Industry and Research Lab Experience

**Naval Research Lab, Radar Division.** (5/1999 to 8/1999, 6/2002 to 7/2003)

Developed high-performance codes for antenna modeling and radar studies.

**Wireless Valley Communications, Inc.** (4/2000 to 8/2001)

Led development of portable measurement platform for in-building wireless communications.

**NASA Langley Research Center** (9/1995 to 8/1998)

Researched hierarchical neural networks for model-based predictive control systems, and built a data acquisition system for magnetic levitation testbed.

## References

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## Citizenship and Clearance

United States citizen

DoD/Secret clearance