Exploiting Parallelism for Improved Automation in Model Order Reduction

Efficient design and verification of systems in mechanics, electronics, biology and several other fields, is often encumbered by the presence of overly detailed models, too complex to be efficiently simulated. These models are the result of overcautious accuracy requirements imposed while representing several subsystems. To tackle this problem, Model Reduction is increasingly becoming a required and common step in most design or analysis methodologies. Model reduction is essentially a mechanism whereby a compressed representation is sought that guarantees appropriate accuracy while preserving relevant model properties. In the context of linear systems, reduction is accomplished by decreasing system order, and a vast alphabet of algorithms has been proposed for this task. Nevertheless, often, more widespread usage of these techniques is thwarted by their lack of automation or outright dependency on user intervention.

In this talk I will discuss algorithms for improving sample point selection in the context of projection-based model order reduction (MOR). Such techniques are fairly general and especially appealing for compression of multi-dimensional parametric models commonly seen in a variety of settings in integrated circuit design. Of particular relevance is the technique’s suitability for parallelization in the context of standard shared and distributed memory architectures. The efficiency speedups achievable with proper mapping of the problem onto parallel hardware enable designers to tackle large and complex models, depending on multiple parameters in an automatic fashion. In addition to the circuit area, which will be covered in this talk, the proposed framework can serve as an essential tool to facilitate fast simulation of large-scale systems in many other application domains such as computational biology and computational neuroscience.

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