Thursday, March 31
Scaife Hall Auditorium
Room 125 at 4:30 p.m.
Refreshments at 4:00 p.m.

Sani Nassif
Manager
IBM Austin Research Laboratory

Sani Nassif received his Bachelor’s degree from the American University of Beirut in 1980, and his Masters and PhD degrees from Carnegie-Mellon University in 1981 and 1985, respectively. He worked at Bell Laboratories until 1996, then joined the IBM Austin Research Laboratory where he currently manages the Silicon Analytics department. He has authored numerous conference and journal publications, received five Best Paper awards (IEEE Trans. CAD, ICCAD, DAC, ISQED and ICCD), authored invited papers to ISSCC, IEDM, ISLPED, HOTCHIPS, and CICC, and given Keynote and Plenary presentations at Sasimi, ESSCIRC, BMAS, SISPAD, SEMICON, PATMOS and VLSI-SOC. He is an IEEE Fellow (2008), a member of the IBM Academy of Technology, a member of the ACM, and is an IBM Master Inventor with more than 40 patents.

The Light at the End of the CMOS Tunnel

In spite of numerous predictions to the contrary, Silicon technology is marching along past the 22nm node and on to ever-finer dimensions. Innovations at the technology, device, circuit and system levels continue to enable us to scale in spite of what sometime appear to be insurmountable problems in power, lack of performance, manufacturability and so on. To a large degree, these innovations are necessary because no substitute technology has been found as yet and, in fact, it does not appear likely that any such technology will become practical this decade. This leaves us with the need to anticipate and predict the near and medium term futures of CMOS for the next handful of technology nodes.

This talk will focus on doing just that, and will show how an important new constraint on future system scaling is circuit resilience. Resilience is the ability of circuits to operate in spite of challenges like noise, difficult environmental conditions, aging and manufacturing imperfections. These factors conspire to cause transient or permanent errors that are indistinguishable from traditional “hard” faults typically caused by defects during fabrication. Without significant innovation at the circuit and system levels, the probability of these events can rise quite dramatically. In the area of SRAM, such phenomena have existed for the last three or four technology nodes, but significant investments in this area have indeed allowed continued system level scaling with ever larger on-chip memories. As these same phenomena start attacking integrated circuits more pervasively, there is an urgent need for research and development in this area to avert the problems certain to arise with increased defect rates.

This seminar explores the link between the old subject of manufacturing variability and its well known impact on circuit performance, and the new subject of the way that same variability -in the extreme- can cause complete circuit failure. With care, we will find that the light at the end of the CMOS tunnel is the opening of new opportunities to enrich CMOS with new technologies like MEMS, optics, sensors and even biological devices. Otherwise, that light is likely to be another train.

ECE Seminar Hosts
Jeyanandh Paramesh
paramesh@ece.cmu.edu
Onur Mutlu
onur@cmu.edu
Gabriela Hug
ghug@ece.cmu.edu
Xin Li
xinli@ece.cmu.edu