Synchronous elastic systems and their extension for modeling and validation of communication fabrics

In this talk we will attempt to cover three somewhat related topics.

We will first review synchronous elastic (aka latency insensitive) systems that have been suggested by a few research groups as a form of a discretized asynchronous system. Such systems are ‘time elastic’ in a sense that they can tolerate dynamic and static changes in latencies of computation and communication components. Therefore, they enable new micro-architectural trade-offs, e.g. a wider use of variable latency components targeting average case optimization, rather than the worst-case optimization traditional to regular synchronous circuits. After introducing principles of designing elastic systems we will discuss the results of a recent design experiment redesigning an H.264 CABAC decoder.

We next describe how to extend the compositional approach of elastic systems to a broader class of designs for the purpose of micro-architectural specification and formal validation. Our focus will stay on communication fabrics -- a critical component for the fast integration and efficiency of operation of the high-end and the SOC products. Avoiding message dependent deadlocks in communication fabrics is critical for modern microarchitectures. However, formal proofs of liveness even on abstract models are hard due to large number of queues and distributed control. We address liveness verification of communication fabrics described in the form of high-level microarchitectural models which use a small set of well-defined primitives (extended from the set of elastic primitives). We prove that under certain realistic restrictions, deadlock freedom can be reduced to unsatisfiability of a system of Boolean equations and automatic generation of inductive invariants. Using this approach, we have automatically verified liveness of several non-trivial models derived from industrial microarchitectures, where state-of-the-art model checkers failed and pen and paper proofs were either tedious or unknown.

Finally, we will address a few design challenges and their implications to CAD problems in architecture and system-level design.