Electrical & Computer ENGINEERING **SEMINAR**

Distinguished Seminar

Thursday, April 29th

Scaife Hall Auditorium
Room 125

4:30 p.m.
Refreshments at 4:00 p.m.

Ulf Schlichtmann
Technische Universität München
Munich Germany

Ulf Schlichtmann is professor at Technische Universität München (TUM) in Munich, Germany, and head of the Institute for Electronic Design Automation at TUM. His research deals with EDA for both digital and analog circuits. The current focus is on statistical design, dealing with aging effects and physical design for digital circuits as well as design centering for analog circuits. Besides his regular teaching, Ulf also is program director of TUM's international M.Sc. program in Communications Engineering and chairman of the Program Management Committee for the M.Sc. program in Integrated Circuit Design conducted jointly by TUM and NTU in Singapore.

Since 2008, Ulf also serves as Dean of TUM's Department of Electrical Engineering and Information Technology.

Prior to his current appointment, Ulf held various technical and management positions during ten years at Siemens and Infineon Technologies. He holds a Dipl.-Ing. degree in electrical engineering and a Ph.D. degree in computer-aided design from TUM. He also obtained a Master's degree in technology business from University of Hagen.

Aging of ICs: Considering it during design in a smarter fashion

The impact of parameter variations on the behavior of ICs has been analyzed for analog ICs since many years. Recently such variations have required more detailed analysis also for digital ICs. While in the past few years the emphasis has been on dealing with manufacturing variations by statistical techniques, now also the degradation of an IC due to aging effects is gaining attention.

I will first motivate why this is relevant by discussing the impact of major aging effects such as NBTI and HCI on circuit performance. Their impact depends on environmental factors as well as on the specific utilization of a transistor. Today, in industrial design flows this impact is only considered via generic safety factors, if at all. To achieve higher analysis accuracy, I will present an aging-aware gate model which allows an accurate analysis of circuit aging on gate level. As a next step, then a hierarchical model is presented that permits a compressed modeling of the timing and aging behavior of an IP block. This model can achieve more than 50x speedup compared to an analysis on gate level and therefore enables an aging analysis on system level. Results on benchmark circuits are presented.

ECE Seminar Hosts

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