Electrical & Computer ENGINEERING **SEMINAR**

Thursday, November 5th
Scaife Hall Auditorium
Room 125
4:30 p.m.
Refreshments at 4:00 p.m.

Professor Borivoje Nikolic
Department of Electrical Engineering
and Computer Science
University of California, Berkeley

Borivoje Nikolic is a Professor of Electrical Engineering and Computer Sciences at the University of California, Berkeley. He received the Dipl.Ing. and M.Sc. degrees in electrical engineering from the University of Belgrade, Serbia, in 1992 and 1994, respectively, and the Ph.D. degree from the University of California at Davis in 1999.

His research activities include digital and analog integrated circuit design and VLSI implementation of communications and signal processing algorithms. He is co-author of the book Digital Integrated Circuits: A Design Perspective, 2nd ed, Prentice-Hall, 2003.

For work with his students and colleagues he has won the best paper awards at the IEEE International Solid-State Circuits Conference, the Symposium on VLSI Circuits, the ACM/IEEE International Symposium on Low Power Electronics and Design and the IEEE International SOI Conference.

SRAM Variability in Space and Time

Increased process and device variability presents a major challenge for future SRAM scaling. Fast and accurate validation of SRAM read stability and writeability margins is crucial for estimating yield in large SRAM arrays. Conventional static SRAM read/write metrics are characterized through test structures that are able to provide limited hardware measurement data and cannot be used to investigate cell bit fails in functional SRAM arrays. As an alternative, distributions of minimum operating voltage (Vmin) are often used to characterize SRAM robustness. This talk reviews our recent work on large-scale characterization of static and dynamic read stability and writeability in functional SRAM arrays using direct bit-line measurements in 45nm CMOS. It also establishes a relationship between the static noise margin distributions and Vmin. The static noise measurement structures are augmented to characterize variability of SRAM robustness in time due to the effects of random telegraph noise (RTS) and bias temperature instability (BTI). The RTS has a small impact on Vmin requirement that can possibly be folded into the BTI design margin.

ECE Seminar Hosts

Jeyanandh Paramesh	paramesh@ece.cmu.edu
Onur Mutlu	onur@cmu.edu
Gabriela Hug	ghug@ece.cmu.edu

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