

Thursday, October 22rd

Scaife Hall Auditorium

Room 125

4:30 p.m.

Refreshments at 4:00 p.m.

**Assistant Professor Subhasish Mitra**Electrical Engineering & Computer Science
Stanford University

Subhasish Mitra is an Assistant Professor in the Department of Electrical Engineering and the Department of Computer Science of Stanford University where he leads the Stanford Robust Systems Group. His research interests include: Robust system design; VLSI design, CAD, validation and test; Design for emerging nanotechnologies. Prior to joining Stanford, Prof. Mitra was a Principal Engineer at Intel Corporation. He received Ph.D. in Electrical Engineering from Stanford University.

Prof. Mitra has co-authored 100+ technical papers, and has invented design and test techniques that have seen wide-spread proliferation in the semiconductor industry. His X-Compact technique for test compression is used by 50+ Intel products, and is supported by major CAD tools. His work on imperfection-immune circuits using carbon nanotubes, jointly with his students and collaborators, has been highlighted "as a significant breakthrough" by the Semiconductor Research Corporation, MIT Technology Review, and several others.

Prof. Mitra's major honors include the Presidential Early Career Award for Scientists and Engineers (PECASE, the highest honor bestowed by the US government on early-career outstanding scientists and engineers), NSF CAREER, Terman Fellowship, ACM SIGDA Outstanding New Faculty Award, IEEE CAS/CEDA Pederson Award for the IEEE Trans. CAD Best Paper, IEEE/ACM Design Automation Conf. Best Paper, Divisional Recognition Award from Intel "for a Breakthrough Soft Error Protection Technology," and the Intel Achievement Award, Intel's highest corporate honor, "for the development and deployment of a breakthrough test compression technology."

Imperfection-Immune Digital VLSI using Carbon Nanotube Field Effect Transistors

Carbon Nanotube Field Effect Transistors (CNFETs), consisting of semiconducting single walled Carbon Nanotubes (CNTs), have several promising applications such as extensions to silicon VLSI. Ideal CNFETs can provide significant energy and performance benefits over silicon-CMOS. However, future gigascale systems cannot rely solely on existing chemical synthesis for guaranteed ideal devices. VLSI-scale logic circuits using CNFETs must overcome major challenges posed by: 1) Mis-positioned CNTs; 2) Metallic CNTs; and, 3) Wafer-scale Integration.

Mis-positioned CNTs can result in incorrect logic functionality of CNFET circuits. A CNT can be semiconducting or metallic depending upon the arrangement of carbon atoms. Metallic CNTs create source-drain shorts in CNFETs resulting in excessive leakage ($I_{on}/I_{off} 10$, i.e., orders of magnitude lower than silicon CMOS) and highly-degraded noise margins.

A combination of design and processing techniques, presented in this talk, enable VLSI-scale CNFET logic circuits that are immune to high rates of inherent imperfections. These techniques are inexpensive compared to traditional defect- and fault-tolerance, do not impose major changes in VLSI design flows, and are compatible with VLSI processing because they do not require special customization on chip-by-chip basis.

Fabrication results will be presented to demonstrate the effectiveness of these techniques in enabling VLSI-compatible imperfection-immune complex CNFET logic gates and circuits.

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