

# SEMINAR

**THURSDAY  
FEBRUARY 14, 2008**

**Scaife Hall Auditorium  
Room 125**

**4:30 p.m.**  
Refreshments—4:00 p.m.

## **DR. MASSOUD PEDRAM**

*PROFESSOR AT THE UNIVERSITY OF SOUTHERN CALIFORNIA*




Joined the EE department of USC after receiving a PhD in EECS from UC-Berkeley in 1991. He was a recipient of the NSF's Young Investigator Award and the Presidential Faculty Fellows Award in 1996. Dr. Pedram, who is best known for his work in low power design, has to date published four books and more than 300 papers, and received four Conference and two IEEE Transactions Best Paper awards. Dr. Pedram is a Fellow of the IEEE and his research currently focuses on energy efficiency and reliability in CMOS VLSI circuits.

**ECE Seminar Hosts:**  
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## **Coarse Grain Power Gating in ASIC Designs Applications**

Power gating, also known as Multi-threshold CMOS, is used to shut down certain power domains in a chip while leaving others active. Power shutdown can significantly reduce leakage power since many applications do not utilize all chip functions at all times. The basic idea of power gating is to separate the VDD or VSS power supply from the standard cells using power switches. The switches can be either PMOS or NMOS transistors that switch VDD or VSS, respectively. This talk focuses on coarse-grain power gating in ASIC designs, which switches entire blocks/rows of standard cells. This choice is due to lower cost and greater leakage savings of coarse-grain power gating compared to its fine-grain counterpart, which inserts the header or footer in each standard cell in the ASIC design library. More precisely, in my talk I will discuss and outline solutions.

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