

DISTINGUISHED LECTURE

**THURSDAY
FEBRUARY 28,
2008**

**LOCATION: SCAIFE 125
TIME: 4:30 P.M.
REFRESHMENTS: 4 P.M.**



Jacob A. Abraham

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Jacob A. Abraham is Professor of Electrical and Computer Engineering and Professor of Computer Sciences at the University of Texas at Austin. He is also the director of the Computer Engineering Research Center and holds a Cockrell Family Regents Chair in Engineering. He received his Ph.D. in Electrical Engineering and Computer Science from Stanford University in 1974.

His research interests include VLSI design and test, formal verification, and fault-tolerant computing. He has published extensively and is included in a list of the most cited researchers in the world. He has supervised more than 60 Ph.D. dissertations, and is particularly proud of the accomplishments of his students, many of whom occupy senior positions in academia and industry. He has served as associate editor of several IEEE Transactions, and as chair of the IEEE Computer Society Technical Committee on Fault-Tolerant Computing.

He has been elected Fellow of the IEEE as well as Fellow of the ACM, and is the recipient of the 2005 IEEE Emanuel R. Piore Award.

Enabling Systems on a Chip to Test Themselves

Advances in semiconductor technology have enabled the integration of digital, mixed-signal, and RF systems on a single chip. While Systems on a Chip (SoCs) offer many benefits in cost and performance, they pose significant challenges for testing after manufacture. This talk will describe a novel approach which uses the computational resources within the SoC to test itself. The embedded processor in the SoC can test itself by running instruction sequences from memory. The tests can target classic "stuck-at" faults as well as small delay defects which are becoming more common in scaled technologies. We have recently developed techniques for generating instruction sequences which have very high coverage for path delay faults in the processor.

The processor can then be used to test other cores in the SoC, including mixed-signal cores for the analog and RF specifications. An approach to testing data converters, by putting them in loopback mode, will be described. On-chip sensors which can be used to test RF modules will also be discussed.

Results of simulations and measurements on prototype hardware show that the approach can predict the specifications of the mixed-signal modules with high accuracy, enabling low-cost manufacturing test.

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