

**THURSDAY
MARCH 29, 2007**

**Scaife Hall Auditorium
Room 125**

**4:30 p.m.
Refreshments—4:00 p.m.**

Interactive Performance Debugging of Real-Time Embedded Systems

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Samarjit Chakraborty received his Ph.D. in Electrical and Computer Engineering from ETH Zurich in 2003. Since then he is an assistant professor of Computer Science at the National University of Singapore. His research interests are broadly in the area of modeling, power/performance analysis and tools for the design of real-time and embedded systems. For his Ph.D. thesis, he received the ETH Medal and the European Design and Automation Association's "Outstanding Doctoral Dissertation Award" in 2004. He also received Best Paper Award nominations at DAC 2005 and CODES+ISSS 2006. Samarjit has served on the technical program committees (TPCs) of a number of premier conferences in the area of real-time and embedded systems (e.g. RTSS, RTAS, RTCSA, ECRTS, DATE and CODES+ISSS) and has extensively published in many of these forums. He will also serve as the TPC co-chair of ESTIMedia 2007 and RTSS 2007 (Hw/Sw Co-design Track). Apart from giving invited lectures at many industrial research labs and universities around the world, Samarjit has also conducted a number of tutorials in the areas of real-time multimedia systems and embedded systems.

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A typical design process for real-time embedded systems involves choosing the values of certain system parameters, followed by a timing/performance analysis to determine whether all design constraints have been satisfied. Such parameters might range from activation rates of different tasks and task deadlines, to task partitioning and mapping decisions. If some of the design constraints fail to get satisfied, one or more system parameters are changed and the analysis is invoked once again. This iteration is repeated in an interactive fashion till a satisfactory design is obtained.

However, it turns out that for most real-life systems, timing/performance analysis is computationally expensive and hence such an interactive performance debugging cycle is very tedious. Further, such designs often involve multiple performance trade-offs and computing the underlying the trade-off or pareto-curve is also a computationally expensive, and often infeasible, procedure.

In this talk I shall describe some of our recent efforts in addressing these problems. In particular, I will outline an "interactive schedulability analysis" algorithm that exploits the fact that with small changes in the system parameters, the full schedulability analysis machinery need not be invoked. This easily leads to more than 20x speedups in the analysis and greatly simplifies the above-mentioned interactive performance debugging cycle. I will also describe a related algorithm that efficiently, but approximately, computes trade-off curves and as a result meaningfully exposes the different performance trade-offs involved in a design.