

**THURSDAY
APRIL 12, 2007**

**Scaife Hall Auditorium
Room 125**

4:30 p.m.
Refreshments—4:00 p.m.

LI-SHUIAN PEH

**ASSISTANT PROFESSOR OF
ELECTRICAL ENGINEERING
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Li-Shuian Peh has been an Assistant Professor of Electrical Engineering at Princeton University since 2002. She graduated with a Ph.D. in Computer Science from Stanford University in 2001, and a B.S. in Computer Science from the National University of Singapore in 1995. Her research focuses on low-power interconnection networks, on-chip networks and parallel computer architectures, and is funded by several grants from the National Science Foundation, the DARPA MARCO Gigascale Systems Research Center as well as Intel Corporation. She was awarded the Sloan Research Fellowship in 2006, and the NSF CAREER award in 2003.

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Towards the Ideal On-Chip Interconnect Fabric

To continue to deliver Moore's Law performance, companies are moving towards multi-core and many-core chips in both general-purpose and embedded domains. While moving from a large monolithic core to a multi-core design will ease the power consumption of the processor cores, the interconnection fabric's power consumption can be substantial and needs to be carefully designed.

In this talk, I'll show the significant power-performance gap that exists between the state-of-the-art interconnection fabric and the ideal interconnect of dedicated wires, and follow on with a discussion of our work to close this gap. Next, I'll discuss our efforts in using the network not just for communications, but for managing on-chip data coherence as well, thereby improving performance beyond that of an ideal interconnect.

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