

**THURSDAY
FEBRUARY 15, 2007**

**Scaife Hall Auditorium
Room 125**

4:30 p.m.
Refreshments—4:00 p.m.

DR. MARCO CACCAMO

**PROFESSOR
UNIVERSITY OF ILLINOIS, URBANA-CHAMPAIGN**



Marco Caccamo is Assistant Professor at Dept. of Computer Science, University of Illinois, Urbana-Champaign. He received a PhD in Computer Engineering from Scuola Superiore Sant'Anna in 2002.

He is the recipient of NSF CAREER Award (2003). His research interests include real-time operating systems, real-time scheduling.

ECE Seminar Hosts:

Radu Marculescu,
radum@ece.cmu.edu
Ken Mai,
kenmai@ece.cmu.edu
Marios Savvides,
Marios.Savvides@ri.cmu.edu

Coscheduling of Software and Hardware Real-Time Tasks for FPGA-based Embedded Systems

Operating systems for reconfigurable devices enable the development of embedded systems where software tasks, running on a CPU, can coexist with hardware tasks running on a reconfigurable hardware device (FPGA). When a real-time system is subject to dynamic workloads and tasks can be computationally intensive, runtime reconfiguration can be used to maximize performance in terms of number of admitted tasks or achieved QoS.

Relocatable tasks can be migrated from software to hardware and vice versa: combination of high performance and predictability of hardware execution with software flexibility makes such architecture especially suitable to implement high-performance real-time embedded systems. In this talk, we introduce a novel resource allocation scheme and admission control test that can be run on-line, thus allowing for highly dynamic scheduling of tasks while maximizing a given performance metric (like the number of admitted tasks). Task allocation and migration between the CPU and the reconfigurable device are analyzed and sufficient feasibility tests are derived. In particular, we show that, by introducing suitable constraints on tasks' parameters, it is possible to efficiently relocate tasks while preserving all real-time requirements of the system at the cost of a bounded overhead on the CPU.

The effectiveness of our admission control and relocation strategy is shown through a series of synthetic simulations.

Finally, a 1D system architecture and its prototype for a Xilinx Virtex-4 FPGA are discussed.