

**THURSDAY
MAY 3, 2007**

**Scaife Hall Auditorium
Room 125**

**4:30 p.m.
Refreshments—4:00 p.m.**

NIRAJ K. JHA

**PROFESSOR OF ELECTRICAL
ENGINEERING
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Niraj K. Jha received his B.Tech. degree in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur, India in 1981 and Ph.D. degree in Electrical Engineering from University of Illinois at Urbana-Champaign in 1985. He is a Professor of Electrical Engineering at Princeton University. He is a Fellow of IEEE and ACM. He has served as the Director of the Center for Embedded System-on-a-chip Design funded by New Jersey Commission on Science and Technology. A textbook he co-authored titled "Testing of Digital Systems" is being used widely around the world. He is the editor-in-chief of TVLSI and serves on the editorial boards of TCAD and TCAS II. He has co-authored seven papers which have won Best Paper Awards. His research interests include nanotechnology, embedded system analysis and design, power/thermal aware hardware/software design, computer-aided design of ICs and systems, computer security, and digital system testing.

ECE Seminar Hosts:

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NATURE: A Hybrid Nanotube/CMOS Dynamically Reconfigurable Architecture

As CMOS technology approaches its physical limits, a tremendous amount of effort is being devoted to nanotechnology research in order to enable future technology scaling. Recent progress on nanodevices, such as carbon nanotubes and nanowires, points to promising directions for future circuit design. However, nanofabrication techniques are not yet mature, making implementation of such circuits, at least on a large scale, in the near future infeasible. However, if photo-lithography could be used to implement circuits using these nanodevices, then hybrid nano/CMOS chips could be fabricated immediately. A startup company called Nantero, has developed and implemented using photo-lithography a non-volatile nano random-access memory (NRAM) that has considerably faster and denser than DRAM, much lower power consumption than DRAM flash, has similar speed to SRAM and is highly resistant to environmental forces (temperature and magnetism). In this talk, we will discuss a high performance reconfigurable architecture, called NATURE, which utilizes CMOS logic and NRAM. Use of highly-dense NRAMs allows sufficient on-chip configuration storage, enabling fine-grained (even cycle-by-cycle) temporal logic folding of a circuit before being mapped to the architecture. This can significantly increase the logic density of NATURE (by over an order of magnitude) relative to traditional reconfigurable architectures, while remaining competitive in performance.

We will also present an integrated design optimization platform for NATURE, called NanoMap. Given a mixed RTL/gate-level design, NanoMap optimizes and implements the design of NATURE through logic mapping, temporal logic clustering, placement, and routing. NanoMap automatically explores and identifies the best temporal logic folding configuration, targeting area, delay, and area-delay product as the optimization objective. Experimental results demonstrate that NanoMap can reduce the area-delay product of a design by over an order of magnitude, and effectively exploits the different features of NATURE.

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