Electrical & Computer ENGINEERING

SEMINAR

THURSDAY
FEBRUARY 2, 2006

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM

MICHAEL SCHULTE

UNIVERSITY OF WISCONSIN-MADISON

Dr. Mike Schulte received a B.S. degree in Electrical Engineering with a second major in Computer Science from the University of Wisconsin-Madison in 1991, and M.S. and Ph.D. degrees in Electrical Engineering from the University of Texas at Austin in 1992 and 1996, respectively. From 1996 to 2002, he was an assistant and associate professor at Lehigh University, where he directed the Computer Architecture and Arithmetic Research Laboratory. In 1997, he received a NSF CAREER Award to research hardware support for accurate and reliable numerical computations. In 2001 and 2004, he received IBM Faculty Partnership Awards for research in high-performance processor design.

Mike is currently an assistant professor at the University of Wisconsin-Madison, where he leads the Madison Embedded Systems and Architectures Group. His research interests include high-performance embedded processors, computer architecture, domain-specific systems, computer arithmetic, and software defined radio. Mike is an associate editor for the IEEE Transactions on Computers and the Journal of VLSI Signal Processing. He has served as the program chair for the IEEE International Conference on Application-Specific Systems, Architectures, and Processors, the Asilomar Conference on Signals, Systems, and Computers, and the IEEE International Symposium on Computer Arithmetic.

A LOW-POWER MULTITHREADED PROCESSOR FOR WIRELESS COMMUNICATION SYSTEMS

Embedded digital signal processors for wireless communication systems have stringent design constraints including high computational throughput, low power consumption, and low interrupt latency. Furthermore, these processors should be compiler friendly, so that code for them can quickly be developed in a high-level language. In this talk, I present the design of a high-performance, low-power digital signal processor for wireless communication systems. The processor uses multithreading, vector processing, and powerful compound instructions to provide real-time baseband processing capabilities with very low power consumption. Using a super-computer class vectorizing compiler, the processor performs complete physical layer processing in real-time for several wireless communication protocols. Instruction set extensions to the processor enable very high bandwidth for several important wireless communication algorithms.

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For more information:
http://www.ece.cmu.edu/seminar

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