

**THURSDAY
OCTOBER 12, 2006**

**Scaife Hall Auditorium
Room 125**

**4:30 p.m.
Refreshments—4:00 p.m.**



Kaushik Roy
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Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently a Professor and holds the Roscoe H. George Chair of Electrical & Computer Engineering. His research interests include VLSI design/CAD for nano-scale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification, and reconfigurable computing. Dr. Roy has published more than 400 papers in refereed journals and conferences, holds 10 patents, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill).

Dr. Roy received the National Science Foundation Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, and best paper awards at 1997 International Test Conference, IEEE 2000 International Symposium on Quality of IC Design, 2003 IEEE Latin American Test Workshop, 2003 IEEE Nano, 2004 IEEE International Conference on Computer Design, and 2005 IEEE Circuits and system society Outstanding Young Author Award (Chris Kim), 2006 IEEE Transactions on VLSI Systems best paper award. Dr. Roy is Purdue University Faculty Scholar. He is the Chief Technical Advisor of Zenasis Inc. and Research Visionary Board Member of Motorola Labs (2002). He has been in the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, and IEEE Transactions on VLSI Systems. He was Guest Editor for Special Issue on Low-Power VLSI in the IEEE Design and Test (1994) and IEEE Transactions on VLSI Systems (June 2000), IEE Proceedings -- Computers and Digital Techniques (July 2002). Dr. Roy is a fellow of IEEE.

**Radu Marculescu,
ECE Seminar Host:**
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Process-Tolerant Low-Power Design for the Nano-meter Regime

Scaling of technology over the last few decades has produced an exponential growth in computing power of integrated circuits and an unprecedented number of transistors integrated into a single. However, scaling is facing several problems – severe short channel effects, exponential increase in leakage current, increased process parameter variations, and new reliability concerns. We believe that *device aware circuit and architecture design* along with *statistical design techniques* can provide large improvement in power dissipation while providing the required reliability and yield. In this talk I will present design techniques to address power and reliability problems in scaled technologies for both logic and memories.