

**FRIDAY
OCTOBER 13, 2006**

HH1112

**10:00am
Refreshments 9:30am**

FREDERICK DILL
HITACHI



Since 1958, when he joined IBM Research Division, then in Poughkeepsie, New York, Dr. Frederick (Rick) Dill, the inaugural recipient of the IEEE Jun-ichi Nishizawa Medal, has done seminal work in a wide range of fields. Dr. Dill's early achievements include essential contributions to semiconductor lasers and to building highspeed integrated circuits using germanium. In the 1970s, he headed research that led to pioneering process models and materials characterization for photolithography. His work helped transform device lithography from an art to an engineering science. His papers are still referenced today, and the parameters used to describe photoresist exposure are called 'The Dill Parameters.' In the 1980s, Dr. Dill was lead inventor of video RAM. Currently, he works on disk drive recording heads to improve their capacity. Today's disk drive heads are built using processes he pioneered.

An IEEE Life Fellow, Dr. Dill has served on the IEEE Board of Directors as Division I Director. He also served as president of the IEEE Electron Devices Society and on the society's Administrative Committee. He helped establish several IEEE journals including the IEEE Journal of Technology--Computer Aided Design, the first IEEE all-electronic journal. Inaugurated into the U.S. National Academy of Engineering in 1990, Dr. Dill subsequently chaired the Academy's Electronics Engineering section. He also was one of the early presidents of IBM's Academy of Technology. A recipient of an IEEE Centennial Medal and an IEEE Third Millennium Medal, Dr. Dill holds more than 30 patents, including fundamental patents on automated tools for thin film measurements.

IBM promoted him to Distinguished Engineer in 2002. He joined Hitachi Global Storage Technologies in San Jose, California, following IBM's sale of the disk drive business. There, he is an executive engineer solving manufacturing process problems.

ECE Seminar Host:
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SPECIAL SEMINAR

Patterning at Nanoscale

Patterning at nanoscale is related to creating useful structures with difficult to work with thin films at the 100 nm and smaller scale. While there is a challenge to produce suitable lithographic images, the problem only starts there. Lithography is only an intermediary in patterning something that is hopefully both useful and reproducible. What will be presented is some background on the patterning of magnetic sensors, how it was done historically, and the introduction of a new polish assisted patterning technique that is a robust process capable of scaling to sizes well below those used today. Although the examples presented will be in the magnetic storage field, the process approach may well be useful in creating other nanostructures as well.