

THURSDAY
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Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



STEVEN REINHARDT

UNIVERSITY OF MICHIGAN—ANN ARBOR

Steven K. Reinhardt is an associate professor of Electrical Engineering and Computer Science at the University of Michigan in Ann Arbor. His research interests include processor and system architectures, memory systems, reliability, and computer system simulation. He has a BS from Case Western Reserve University and an MS from Stanford University, both in electrical engineering, and a PhD in computer science from the University of Wisconsin-Madison.

Babak Falsafi, ECE Seminar Host
babak@ece.cmu.edu

For more information:
<http://www.ece.cmu.edu/seminar>

INTEGRATING HIGH-BANDWIDTH NETWORKING INTO MODERN ARCHITECTURES

Internet communication is as fundamental as computation in modern computer systems. Nevertheless, network interface controllers (NICs) are typically added on to systems as generic I/O devices. The resulting loose coupling between the NIC and the rest of the system is a significant impediment to utilizing the 10 Gbps Ethernet links now available. The "TCP offload" approach, being pursued by industry, tolerates this bottleneck by moving intelligence to the NIC. We are investigating an alternate approach: addressing the bottleneck directly by integrating an Ethernet NIC on the processor die. This integration not only allows lower latency access from the CPU, but opens the door to treating the NIC as a first-class component of a holistic system design.

Analyzing the performance of alternative system architectures for TCP/IP communication is a significant challenge. We have developed a full-system simulation environment, called M5, capable of simulating client and server systems along with a network in a single process. Simulation results show that a simple on-chip NIC can allow a system to achieve higher bandwidths at lower CPU utilizations than off-chip interfaces. The interaction of the NIC with the on-chip memory hierarchy also has a significant impact.

This talk will cover our current work and future directions in integrated NIC architectures. I will also briefly describe the M5 simulation environment and discuss some of the unique challenges of modeling TCP/IP-intensive workloads.