

THURSDAY
SEPTEMBER 15, 2005

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



YI LUO

ELECTRICAL AND COMPUTER ENGINEERING
CARNEGIE MELLON UNIVERSITY

Yi Luo received a B.S. in 1987 from the University of Science and Technology of China, HeFei, China. From 1990 to 1993, he studied in the Physics Department at the University of Toledo. His MS thesis was on pulsed laser deposition for the growth of II-VI compound semiconductor heterojunctions.

From 1993 to 2000, he studied in the Department of Applied Physics at Columbia University under the advice of Prof. Richard M. Osgood, Jr. His research was focused on low temperature atomic layer epitaxy (ALE) of semiconductors, and detailed surface chemical investigations of metal-organic precursors on semiconductor surfaces in an UHV environment. He received his Ph.D. in March, 2000. From March, 2000 to July, 2005, He had been working in Prof. Jim Heath's group, first as a postdoc and later as a staff scientist at UCLA and then at Caltech. During this period, his research was focused on molecular electronic systems and other novel nano-scale systems for sensing and biological applications.

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For more information:
<http://www.ece.cmu.edu/seminar>

BUILDING NANO-SCALE ELECTRONIC SYSTEMS WITH MOLECULES

First, I will present results from a comprehensive study of a molecular electronic system using bi-stable molecules and nanowires crossbar circuits for memory and logic applications. These include design, fabrication, and characterization of chemical materials, switching devices, and multifunctional circuits. I will show how electrical switching can be accomplished in tunneling junction devices by utilizing chemical bi-stability of molecules. Important issues in fabrication and electrical characterization will be discussed. I will also talk about recent efforts of building a 1MBit memory device at a density of $10^{11}/\text{cm}^2$.

Then, I will discuss some of the fundamental issues and fabrication challenges that we will face as the channel length in a CMOS transistor is being scaled down to $\sim 10\text{nm}$ within a decade or so. The difficulties in current technology promote researches for alternative systems that will play important roles in the future nanoelectronics beyond CMOS. I will introduce methods of fabricating structures, of which critical feature sizes are less than 10nm , and a proposal of building fast and energy efficient single-molecule-transistors on this length scale.