

THURSDAY
NOVEMBER 3, 2005

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



JOHN P. SHEN
DIRECTOR,
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AT INTEL

John P. Shen is the director of the Microarchitecture Research Lab (MRL) at Intel. MRL consists of a couple dozen researchers spread out at three Intel sites in CA, OR, and TX. Prior to joining Intel in 2000 he spent quite a few years as a Professor in the ECE Department at Carnegie Mellon University. He supervised a total of 17 PhD students, published about 100 papers, and received multiple teaching awards, during his years at CMU. He recently published the book "Modern Processor Design: Fundamentals of Superscalar Processors" with McGraw-Hill. He misses academia, but is enjoying his current job in the "real world."

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For more information:
<http://www.ece.cmu.edu/seminar>

IRON LAWS FOR MULTI-CORE SCALABILITY

The current multi-core trend is the new rage in the industry. All major microprocessor companies have introduced or will soon introduce products containing multiple cores on a single die. It seems that scaling the number of cores has replaced the scaling of clock frequency as the primary design objective for architects. How far can we go in scaling the number of cores in the coming decade? What are the foundational principles, or "iron laws," that actually govern the scaling of multi-core machines? What are the fundamental forces that might conspire against multi-core scalability? This talk will attempt to formulate a clean framework to reason clearly about multi-core performance scalability issues. Iron laws on multi-core scalability with respect to architecture, algorithm, and power scaling, will be presented and illustrated with experimental data from MRL's research projects. Speculation on future multi-core designs and promising research directions will also be divulged.