

THURSDAY
MARCH 4, 2004

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



Rajesh Gupta

UNIVERSITY OF CALIFORNIA—SAN DIEGO
COMPUTER SCIENCE AND ENGINEERING

Rajesh Gupta (BTech/EE, IIT Kanpur; MS/EECS, UC Berkeley; PhD/EE Stanford) is the Qualcomm chair professor in Computer Science and Engineering at UC San Diego. His current research interests are in embedded systems and low power design. Earlier, he was on the faculty of Computer Science departments at UC Irvine and University of Illinois, Urbana-Champaign. He is author/co author of over 125 articles on various aspects of embedded systems and design automation and four patents on PLL design, data-path synthesis and system-on-chip modeling. Gupta is editor-in-chief of IEEE Design & Test of Computers and serves on the editorial boards of IEEE Transactions on CAD and IEEE Transactions on Mobile Computing. Gupta is a Fellow of the IEEE and a distinguished lecturer for the ACM/SIGDA and the IEEE CAS Society.

ARCHITECTING EMBEDDED MICROSYSTEMS

As semiconductor processing evolves, the capability to manufacture complex chips vastly outstrips our ability to correctly design these chips in a limited time. Availability of cores, or pre designed specialized function cells such as microprocessors, RF components, network interfaces, encryption and compression engines, holds promise for building systems on a single-chip, thus expanding the reach of silicon into new applications and application domains. Computing elements in these systems can be used to deliver diverse functionality, build and manage mobility, enable energy and location awareness, improve system performance, improve testability and reliability of these systems by adapting to application needs. A good systems engineering, especially for single-chip implementations, requires effective abstraction and reuse of hardware and software components, as well as novel capabilities in the embedded system software.

In this talk, I will present the design of a component composition framework that enables the system architect to interactively explore intelligent design options without leaving the application development environment. We will then discuss our implementation of energy awareness in the embedded system software and how it can be used to do effective management of energy and performance by turning the right hardware and subsystem knobs based on the application context and dynamically changing performance/quality requirements.

While very much a work-in-progress, this research is exciting both theoretically as well as for its potential impact. Formally, the problem of IP modeling and compositional correctness is an open issue that requires fundamental rethinking of the capabilities a high-level language, such as SystemC, provides (by means of static type checking), as well as its relationship to validation tools (both static as well as dynamic verification through assertions).

For more information:

<http://www.ece.cmu.edu/seminar/index.php>

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