

THURSDAY
OCTOBER 14, 2004

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



Joseph Ingino

*SENIOR PRINCIPAL SCIENTIST,
BROADCOM CORPORATION*

Joseph Ingino received the Ph.D. degree in Electrical Engineering from Stanford University in 1998, where his research focused on adaptive calibration techniques for high-speed, high-resolution A/D converters. He is currently a Senior Principal Scientist at Broadcom Corporation where his work focuses on a wide range of analog issues for high-speed communication systems including PLL, CDR, SERDES, and A/D converter designs.

In 1994 he was with AT&T Bell Laboratories working on A/D converters and RF designs for cellular applications.

In 1995 he was with National Semiconductor, where he helped design cellular handsets. From 1998 to 2000 he was with SiByte, a startup company in Santa Clara, CA that was acquired by Broadcom in 2000. There he designed analog blocks, including PLLs, DLLs, and high-speed I/O for network processor SOCs. He has also consulted for a number of companies.

He has published multiple conference and journal articles and is a frequent speaker for the IEEE Solid-State Circuits Society. He has more than 10 patents granted or pending.

Patrick Yue, ECE Seminar Host
cpyue@ece.cmu.edu

For more information:
<http://www.ece.cmu.edu/seminar>

ISSUES IN PHASE-LOCKED LOOP AND CDR DESIGN FOR SOC APPLICATIONS

The trend towards digital systems-on-a-chip (SOCs) with greater levels of integration, higher data rates, and lower supply voltages, has resulted in an increasingly noisy environment in which sensitive circuit blocks, such as phase-locked loops (PLLs), must operate. Noise levels have been further exacerbated by the failure of I/O voltage levels to scale at a rate equal to that of internal core voltages. Moreover, the trend towards higher clock and data rates in digital and mixed-signal SOCs has resulted in more stringent timing margins, primarily in the forms of duty-cycle control and jitter limits. These factors have resulted in increasing demand for high-accuracy PLLs, CDRs (clock and data recovery), and other clock-generating/recovery blocks.

On large SOCs, power-supply noise is often the most common and dominant source of jitter or phase-noise on a PLL's output clock. Jitter can be minimized with careful design of the noise sensitive blocks, such as VCO, in conjunction with regulating the supply to these critical blocks. This talk describes the various tradeoffs and issues related to the design of PLLs for clock synthesis and clock and data recovery. A PLL that achieves a power-supply-rejection ratio (PSRR) greater than 40 dB while operating up to 6 GHz will be described. The PLL is intended for use in a high-speed SOC that operates at internal clock frequencies exceeding 2 GHz. The high level of noise rejection is achieved with a high-bandwidth voltage regulator that provides a nominally noise-free supply to the PLL's sensitive analog blocks. Previous PLL designs have employed voltage regulators to filter out supply noise but have generally been limited to PSRRs of less than 25 dB.