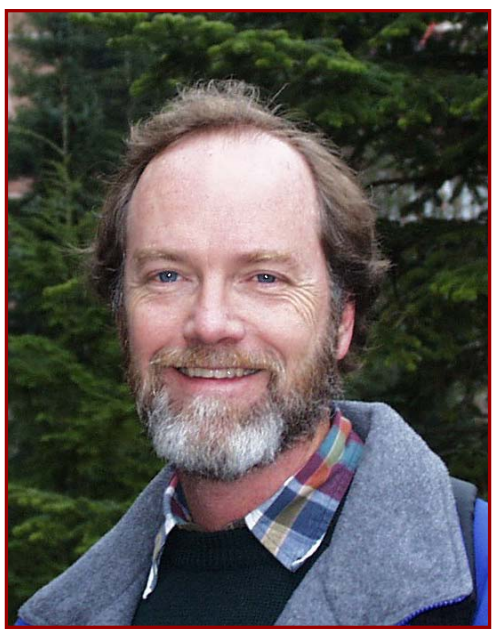
Electrical & Computer ENGINEERING

SEMINAR

THURSDAY
NOVEMBER 6, 2003

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



Carl Ebeling

UNIVERSITY OF WASHINGTON

Carl Ebeling received a Ph.D. in computer science from Carnegie-Mellon University in 1986 and joined the faculty of the University of Washington, where he is currently professor of Computer Science and Engineering. His research interests fall in the area of application-specific VLSI architectures, configurable computing, and computer-aided design of complex digital systems. His current research is focused on architectures, programming and compiling for coarse-grained configurable architectures. In an earlier life, he designed the Hitech chess machine and wrote the Gemini layout-to-schematic comparison program.

COARSE-GRAINED CONFIGURABLE ARCHITECTURE

Much research effort has been spent exploring configurable architectures as a viable component technology for the performance and power demands of programmable platforms for mobile and embedded applications. Configurable architectures achieve high performance using the ability to dynamically configure a hardware solution that takes advantage of the fine-grained parallelism in an application. Low power is achieved using the ability to perform computations with a minimum of data movement, intermediate memory accesses and control.

Most of this research is based on fine-grained FPGAs that are commercially available. Such FPGAs must be applicable across a virtually unlimited range of applications and as such must be infinitely flexible. However, most applications of interest do not leverage the flexibility of these fine-grained FPGAs. By specializing to a narrower domain of application, coarse-grained architectures can attain much larger efficiencies than FPGAs at the expense of generality.

We view coarse-grained configurable architectures as combining features of both FPGAs and traditional microprogrammed architectures like VLIWs. I will first describe a specific instance of such an architecture called Rapid, developed at the University of Washington. Then I will focus on the problem of specifying and compiling algorithms for general coarse-grained configurable architectures using techniques borrowed from both traditional VLIW instruction scheduling and physical circuit design tools.

For more information:
http://www.ece.cmu.edu/index.php

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