

THURSDAY
OCTOBER 16, 2003

Scaife Hall Auditorium
Room 125

4:00 PM
Refreshments—3:30 PM



André DeHon

CALIFORNIA INSTITUTE OF TECHNOLOGY


André DeHon received S.B., S.M., and Ph.D. degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1990, 1993, and 1996 respectively. From 1996 to 1999, André co-ran the BRASS group in the Computer Science department at the University of California at Berkeley. Since 1999, he has been an Assistant Professor of Computer Science at the California Institute of Technology.

André is broadly interested in how we physically implement computations from substrates, including VLSI and molecular electronics, up through architecture, CAD, and programming models. He places special emphasis on spatial programmable architectures (e.g. FPGAs) and interconnect design and optimization.

SUB-LITHOGRAPHIC SEMICONDUCTOR COMPUTING SYSTEMS

How can we build nanometer scale computing devices?

Enabled by advances in our basic scientific understanding at the molecular and atomic scales, we can now engineer designed nanostructures without using lithography. Key features can be a few nanometers wide—a few silicon atoms wide, perhaps the ultimate scale for devices. This will allow us to design computing components without the costs or limits of ultra-fine lithography. Design at this scale, however, will not simply be an extension of our familiar VLSI design. We may not be able to directly pattern complex features, but rather must exploit basic physical properties to define feature sizes, self-assembly to create ordered devices, and post-fabrication reconfigurability to define functionality and mask defects. This creates new challenges for design and exposes a different cost structure which motivates different computing architectures than we found efficient in conventional, lithographically patterned silicon.

I will review the emerging nanoscale fabrication building blocks, sketch a hybrid fabrication scheme which uses these building blocks along with lithography, and present a plausible architecture for nanoscale electronics based on silicon nanowires. I demonstrate that these nanoscale constructs are sufficient to provide universal logic functionality with all logic and signal restoration operating at the nanoscale. 

For more information:

<http://amp.ece.cmu.edu/ECESeminar>

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