Thurs., Sept. 19th
Scaife Hall Auditorium
Room 125 at 4:30 p.m.
Refreshments at 4:00 p.m.

Eriko Nurvitadhi, PhD
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Eriko Nurvitadhi is a researcher in the Intel Science and Technology Center for Embedded Computing (www.istc-ec.org). His research interests are at the intersection of computer architecture, design automation, and reconfigurable logic (FPGAs). Eriko has a PhD in Electrical and Computer Engineering from Carnegie Mellon University and an MBA from Oregon State University.

Compiling Graph Algorithms for Accelerator Platforms

Many emerging applications (e.g., stereo matching, handwriting recognition) in machine learning and data mining can be cast as graph algorithms. Efficient low-power implementations of these graph algorithms promise disruptive capabilities for the increasingly ubiquitous mobile and embedded platforms (e.g., tablets, smart phones, etc). The tight power and cost budgets of these embedded systems, coupled with their stringent real-time performance requirements, are best satisfied through special-purpose hardware acceleration.

This talk will present the GraphGen project from the Intel Science and Technology Center for Embedded Computing at CMU. GraphGen is a domain-specific compiler that compiles graph algorithms described in a widely used vertex-centric graph specification to target a diverse range of accelerator platforms (FPGAs, GPUs). GraphGen compiler provides application-level and algorithm-level developers the ability to take advantage of hardware acceleration for performance and energy efficiency, without being bogged down by low-level hardware development intricacies.