Thursday, Jan. 17th
Scaife Hall Auditorium
Room 125 at 4:30 p.m.
Refreshments at 4:00 p.m.

Dr. Tong Zhang
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Dr. Tong Zhang is an associate professor in Electrical, Computer, and Systems Engineering department at Rensselaer Polytechnic Institute, NY. He joined Rensselaer Polytechnic Institute as an assistant professor in 2002 right after he got his doctoral degree from the University of Minnesota. He co-authored over 120 refereed papers in the areas of memory circuits and systems, VLSI signal processing, and computer architecture, with the total citation of over 1500. He has graduated 12 PhD students all of whom are working in leading-edge semiconductor and data storage companies in US. He currently serves as an Associate Editor for the IEEE Transactions on Circuits and Systems - II and the IEEE Transactions on Signal Processing. He is the technical program co-chair of 2012 ACM Great Lakes Symposium on VLSI and 2012 IEEE Workshop on Signal Processing Systems (SiPS): Design and Implementation. He is a Senior Member of IEEE. He currently serves on the Technical Advisory Board of Skyera Inc., a Silicon Valley startup focusing on next-generation enterprise solid-state data storage systems.

Circuits & Systems for Solid-State Data Storage:
A New Cross-disciplinary research frontier

As a shining spotlight of global semiconductor and computing industry, solid-state data storage using NAND flash memory receives increasingly significant amount of attentions. It has been predicted that solid-state data storage has the potential to become a $100 billion/year market by the close of this decade. Beyond mobile and personal computing devices, future growth of solid-state data storage is primarily attributed to its potential to fundamentally change the memory and storage hierarchy for virtually the entire information technology infrastructure, especially high-end systems such as enterprise computing, data centers, and cloud computing/storage, etc. This grand industry trend and popular optimism are fundamentally based on two widely accepted assumptions: (1) the bit cost of NAND flash memory will continue to drop through and beyond this decade, and (2) people can always build flash-based data storage systems with sufficient reliability and speed performance. The steady bit cost reduction of NAND flash memory is due to the continuous semiconductor technology scaling. However, aggressive technology scaling inevitably leads to continuous degradation of NAND flash memory device quality, which poses significant challenges to reliable and high-speed solid-state storage system design. We believe that, in order to best tackle this challenge, a transition toward more integrated closed-loop design practice is inevitable, which demands true cross-layer cross-disciplinary research innovations. At Rensselaer, we have been actively exploring this new cross-disciplinary research frontier, and in this talk I will report our recent representative work that aims to address the challenge of reliable and high-speed solid-state data storage system design by cohesively leveraging knowledge and techniques across semiconductor device, memory circuits, digital signal processing, error correction coding, information theory, and data storage systems.