Second Workshop on Dependable and Secure Nanocomputing

Friday June 27, 2008, Anchorage, AK, USA **www.laas.fr/WDSN08**

Organizers: **Jean Arlat, LAAS-CNRS, Université de Toulouse, France**
Cristian Constantinescu, AMD, Fort Collins, CO, USA
Ravishankar K. Iyer, UIUC, Urbana-Champaign, USA
Michael Nicolaïdis, TIMA, Université de Grenoble, France

Preliminary Program

9:00 - 10:30

Session 1
Opening and Defect & Failure Modes in Nanoscale Technologies

1a Introduction and Invited Talk
Moderator: TBD

- Invited Talk: The information is not confirmed yet. Sorry for the inconvenience.
  Please visit the Workshop website (www.laas.fr/WDSN08) for most up to date information.

1b Defect and Fault Models in Nanoscale Technologies
Moderator: TBD

- Developing Fault Models for Nanowire Logic Circuits
  Daniel Gil, David de Andrés, Juan-Carlos Ruiz, Pedro Gil — Universidad Politécnica de Valencia, Spain
- SER Characterization of an Advanced Network Processor using Accelerated Neutron Beam
  Nelson Tam[1], ShiJie Wen[2], Noam Lewis[3], Richard Wong[2], Armen Karapetov[4], Oded Rozenstein[4], Haim Boot[3], Reuven Cohen[3], Usama Nassir[1] — [1] Marvell Semiconductor, Inc., Santa Clara, CA, USA; [2] Cisco Systems, San Jose, USA, [3] Marvell Israel Ltd, Yokneam, Israel ; [4] EZchip Technologies Ltd., Yokneam, Israel
- Modeling Microprocessor Faults on High-Level Decision Diagrams
  Raimund Ubar, Jaan Raik, Artur Jutman, Maksim Jenihhin — Tallinn University of Technology, Estonia; Martin Instenberg, Heinz-Dietrich Wuttke — Ilmenau Technical University, Germany

10:30 - 11:00 ***Coffee Break***

11:00 - 12:30

Session 2
Performance and Security Issues in Hardware Design

2a Asynchronous Circuits
Moderator: TBD

- Performance Comparison between Self-timed Circuits and Synchronous Circuits Based on the Technology Roadmap of Semiconductors
  Masashi Imai, Takashi Nanya — The University of Tokyo, Japan
- Concurrent Fault Detection for Secure QDI Asynchronous Circuits
  Konrad J. Kulikowski, Mark G. Karpovsky, Alexander Taubin, Zhen Wang — Boston University, MA, USA

2b Intrusion Detection Devices
Moderator: TBD

- Hardware Implementation of Information Flow Signatures Derived via Program Analysis
  Paul Dabrowski[1], William Healey[1], Karthik Pattabiraman[1], Shelley Chen[2], Zbigniew Kalbarczyk[1], Ravishankar K. Iyer[1] — [1] University of Illinois at Urbana-Champaign, USA; [2] SAIC, Champaign IL, USA
- Low-Cost Self-Test of Crypto Devices
  G. Di Natale, M. Doulcier, M. L. Flottes, B. Rouzeyre, LIRMM, Université de Montpellier, France
- Quantum Wireless Intrusion Detection Mechanism
  Tien-Sheng Lin[1,2], I-Ming Tsai[1], Sy-Yen Kuo[1] — [1] National Taiwan University, Taipei, Taiwan; [2] Lan Yang Institute of Technology, Ilan, Taiwan

12:30 - 14:00 ***Lunch***

14:00 - 15:30

Session 3
Mitigation and Resilience Techniques for Nanocomputing

3a Fault Tolerance Techniques
Moderator: TBD

- Blocking and Non-blocking Checkpointing and Rollback Recovery for Networks-on-Chip
  Claudia Rusu[1], Cristian Grecu[2], Lorena Anghel[1] — [1] TIMA, Université de Grenoble, France; [2] University of British Columbia, Vancouver, Canada
- No Free Lunch in Soft Error Protection?
  Ilia Polian[1], Sudhakar M. Reddy[2], Irith Pomeranz[3], Xun Tang[2], Bernd Becker[1] — [1]Albert-Ludwigs-University, Freiburg, Germany; [2]University of Iowa, Iowa City, USA; [3]Purdue University, West Lafayette, USA

3b Reconfigurable Nanoscale Circuits
Moderator: TBD

- Fault Tolerance of the Input/Output Ports in Massively Defective Multicore Processor Chips
  Piotr Zając[1,2], Jacques Henri Collet[1], Jean Arlat[1], Yves Crouzet[1] — [1] LAAS-CNRS, Université de Toulouse, France ; [2] Technical University of Lodz, Poland
- BISM: Built-in Self Map for Crossbar Nano-Architectures
  Mehdi Tahoori — Northeastern University, Boston, MA, USA
- Combined Defect and Fault Tolerance for Reconfigurable Nanofabrics
  David de Andrés, Juan-Carlos Ruiz, Daniel Gil, Pedro Gil — Universidad Politécnica de Valencia, Spain

3c Workshop Wrap up
Moderator: TBD

15:30 - 16:00 ***Coffee Break***