Tutorial 6

Soft Errors: Technology Trends, System Effects, and Protection Techniques

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Radiation-induced soft errors are getting worse in digital systems manufactured in advanced technologies. Stringent data integrity and availability requirements of enterprise computing and networking applications demand special attention to soft errors in sequential elements and combinational logic. This tutorial will discuss the impact of technology scaling on soft error rates, circuit-level modeling of soft errors, architectural impact of soft errors, challenges associated with evaluation of run-time behaviors of systems in the presence of soft errors, actual data on system behaviors in the presence of soft errors, metrics for quantifying soft error vulnerabilities, design of architectures with Built-in-Soft-Error-Resilience techniques, and actual case studies. Two of the presenters co-founded a new workshop on soft errors (SELSE 2005-2007). Lessons learnt from these workshops will also be included in the tutorial.

Targeted audience: Researchers and practitioners interested in reliable systems modeling, architecture, design, CAD.

About the speakers

Subhasish Mitra is an Assistant Professor in the Departments of Electrical Engineering and Computer Science of Stanford University. His research interests include robust system design, VLSI design and test, computer architecture and design for emerging nanotechnologies. Prior to joining Stanford, he was a Principal Engineer at Intel Corporation where he developed enabling technologies for robust system design – Design for Excellence (Reliability, Testability, and Debug) – that have been deployed in several products. He received Ph.D. in Electrical Engineering from Stanford University.

Prof. Mitra has co-authored more than 90 technical papers and several patents, and invented design and test techniques that have seen wide-spread proliferation in the chip design industry. His X-Compact technique for test compression is used by major (more than 40) Intel products including microprocessors, chipsets, and communications chips, and is supported by major CAD tools. His recent work on imperfection-immune circuit

design using carbon nanotubes, jointly with his students and collaborators, has been highlighted in the MIT Technology Review, EE Times, and several other publications. Prof. Mitra's major honors include the National Science Foundation CAREER Award, Terman Fellow at Stanford University, IEEE Circuits and Systems Society Donald O. Pederson Award for the best paper published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, a Divisional Recognition Award from Intel "for a Breakthrough Soft Error Protection Technology," a Best Paper Award at the Intel Design and Test Technology Conference for his work on Built-In Soft Error Resilience, and the Intel Achievement Award, Intel's highest corporate honor, "for the development and deployment of a breakthrough test compression technology that improved scan test cost by an order of magnitude." Prof. Mitra has held several consulting positions, and served on the committees of several IEEE and ACM sponsored conferences and workshops as co-founder, general and program chair, and organizing and program committee member.

Pia Sanda received the Ph.D. degree in physics from Cornell University, Ithaca, NY, in surface Raman scattering. She was a Manager in the VLSI Design Area, IBM T. J. Watson Research Center, Yorktown Heights, NY. She began her career at IBM in imaging science. In silicon technology, she designed and built 0.1-$\propto$m channel length CMOS FET's using phase shift lithography and contributed to the device and cell design for the 256-Mb DRAM. She has been engaged in designing high-performance circuits for microprocessors and has recently explored new avenues for test and improved semiconductor manufacturability, such as the new PICA measurement technique. She is currently the Program Director of Soft Error Management at IBM.