Rethinking ASIC Design & SRAM Compilation in 14 nm CMOS

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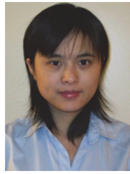
Qiuling Zhu

Larry Pileggi

Below the 32nm node, lithographic patterning and process integration challenges are limiting the ability to scale critical pitches by a full 70%, a metric that was traditionally considered imperative to justify the economics of scaling. These challenges are further aggravated by the need to introduce several new technology elements such as FINFET devices, local interconnects and multiple patterned critical design levels. With process technology being strongly limited by physics and cost, it is necessary to explore other features and opportunities that can make scaling affordale. As part of a DARPA project on Gratings of Regular Arrays and Trim Exposures for digital designs (GRATEdd) with IBM, we have proposed fundamental changes to the standard cell architecture and SRAM compilation methodologies.

For standard cells, we have developed unidirectional-metal1 based standard cells that have comparable design efficiency and superior manufacturability, robustness and scalability compared to traditional bidirectional-metal1 cells. For embedded SRAMs, we have demonstrated that the regular patterning of logic cells and bitcells allows us to synthesis smart SRAM blocks, rather than compile (floorplan hard IP) traditional SRAM blocks with equal robustness.

Preliminary results for the synthesis of smart memory blocks for a 2-port (1R/1W) SRAM and a high throughput interpolation memory demonstrate orders of magnitude savings in power, performance and area as compared to an ASIC block built using SRAM from more traditional SRAM block compilation.

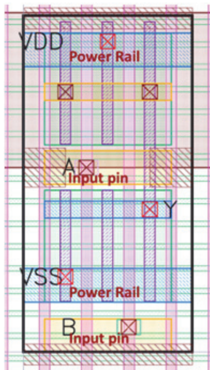

Fig. 1: Unidirectional-Metal1 Standard Cell

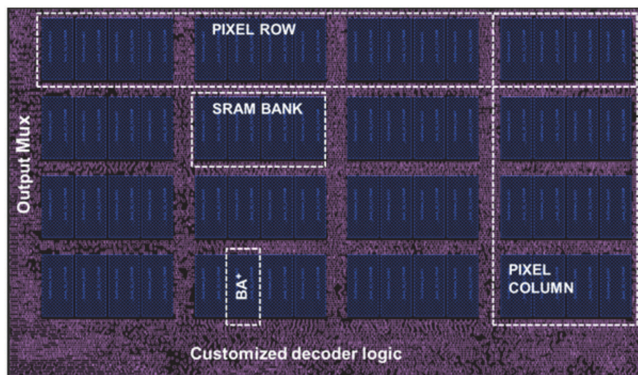

Fig 2: Application-Specific Smart SRAM for Parallel Accesses of a 4x4 Window Block from a 64x64 2D Image Array