Feasibility Study of VeSTICs

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Vertical Slit Field Effect Transistors-based Integrated Circuits (VeSTICs) have been investigated by international team of researchers for last 4 years. (List of co-founders of the VeSTICs Research Team one can be found at www.vestics.org). A pair of complementary junction-less transistors called VeSFETs (Vertical Slit Field Effect Transistors), which is a centerpiece of VeSTICs vision is shown in Fig. 1. Regular array of VeSFETs, such as one shown in Fig. 2, is used as a "canvas" of VeSTICs, which are "customized" with metal interconnect (not shown in Fig 2.)

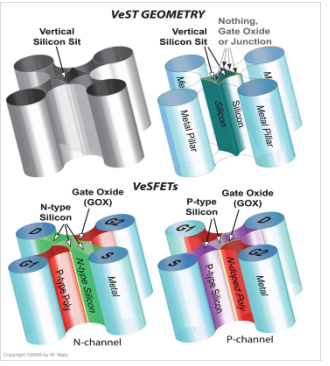

Fig. 1: N and P-channel VeSFETs.

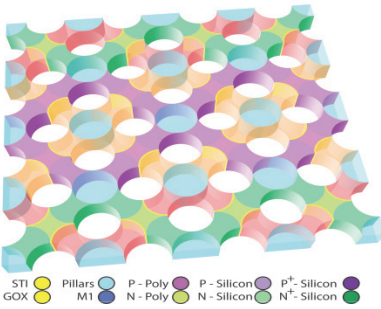

Fig.2: VeSTIC canvas.

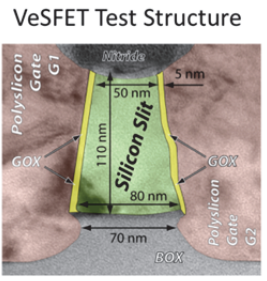

Fig. 3: TEM of VeSFET's slit

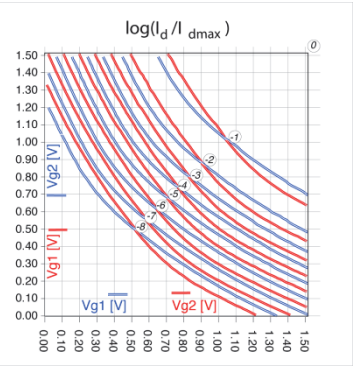

Fig.4: Measured ID (Vg1,Vg2) .

Recently obtained manufacturing results (samples shown in Figs. 3 and 4) confirmed many of highly attractive characteristics of VeSTICs. Thus, we claim that the concept of maximally repetitive VeSTICs canvas, has a potential to provide huge, never-before-available design flexibility together with extreme transistor density both dramatically-increasing levels of manufacturability. However, this cannot be proven unless we identify an industrial partner who will be willing to take a big risk but with substantial chances for much bigger reward.