A Fast Multiscale, Multiphysics CMP Model for CAD Integration

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Since nanoscale integrated circuit (IC) devices are increasing in complexity and systematic variation, there is a greater need for fast, physics-based modeling of manufacturing processes, namely chemical mechanical polishing (CMP). CMP has significant influence on interconnect resistance and changes in coupling and capacitance, which can lead to significant variations in timing and power. The literature shows that CMP defects can lead to short and open circuits. To date, empirical-based CMP models have aided IC designers by way of design rules. However, design rules for chips sub-22 nm will either be low-yielding or overly conservative. Therefore, there is a need for introducing multi-physics CMP modeling into the computer aided design (CAD) framework, without adding prohibitive computational times to the design cycle.

Our work aims to demonstrate the feasibility of introducing a multi-scale (i.e., feature, die and wafer scale), multi-physics CMP model into a CAD framework by employing highly parallelized computational methods and numerically optimized physics treatments. We have recently developed a faster, chip- to wafer- scale, physics-based CMP model which leverages our multiphysics modeling framework known as particle-augmented mixed lubrication (PAML). This faster PAML, known as "PAML-lite" is being integrated into the CAD flow to predict the polish rate and surface topography evolution to quantify variation (Fig 1). Reductions in computation times are being researched by parallelizing our multi-physics algorithms on the Pittsburgh Supercomputers and graphic processing unit (GPU) platforms via CUDA. CUDA, a parallel computing architecture which utilizes the inherently multi-core GPU, has shown significant speedups (see Fig. 2) An advantage of our methodology is that this approach would continue to hold as technology scales and with increasing layout regularity.

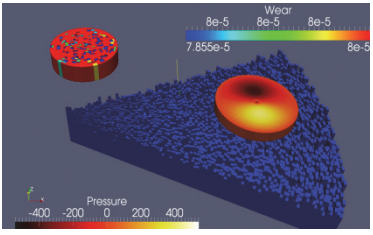

Fig. 1: Wafer scale physics-based CMP modeling

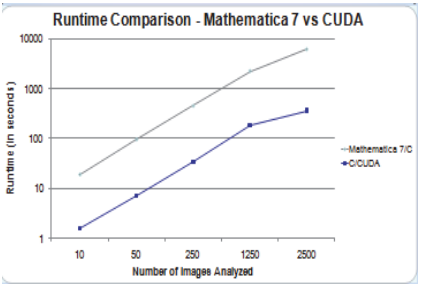

Fig 2: Computational runtimes for existing CMP model vs. a CUDA-enabled CMP model