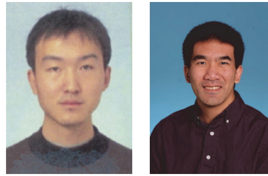
Error Patterns in MLC NAND Flash Memory: Characterization and Analysis



Yu Cai **Ken Mai**

As NAND flash memory manufacturers scale down to smaller process technology nodes and store more bits per cell, reliability and endurance of flash memory is becoming a significant concern. Wear-leveling and error correction coding can improve both reliability and endurance, but finding effective algorithms requires a thorough understanding of flash memory error patterns. To enable such understanding, we have designed and implemented an FPGA-based framework for fast and accurate characterization of flash memory throughout its lifetime. This work examines flash errors characteristics at 40nm and below flash technologies.

We characterize and analyze errors in modern flash memory from flash controller's point of view, categorizing them into four types: erase errors, program interference errors, retention errors, and read errors. We find that (1) all types of errors are highly correlated with P/E cycles; (2) the long-term retention errors are the most dominant and the program interference error rate ranks second; (3) retention error rates are highly dependent on retention test time. We also uncover distinct error patterns, such as cycle-dependency, location dependency and value-dependency, for various types of flash operations. The asymmetry of retention errors and program errors are shown in Figure 2. All these discovered error patterns can be explained from a circuit and device standpoint. The understanding developed from this characterization serves as a building block for new error tolerance algorithms for flash memory based data storage.

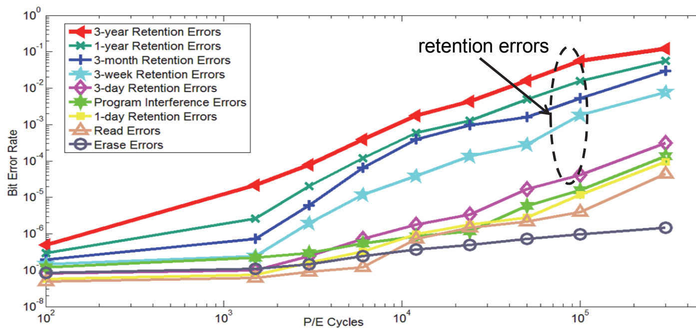


Fig. 1: Rates of various types of errors as P/E cycles increase.

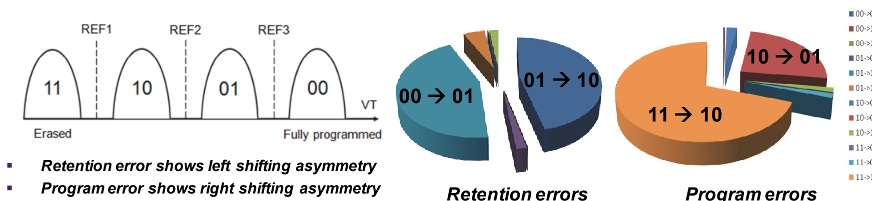


Fig. 2: Asymmetry of retention errors and program interference errors.