

High Mobility Graphene Electronics



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Graphene, a monolayer of carbon arranged in a hexagonal lattice, is a material that has received considerable attention from the scientific community due to its remarkable characteristics. In electronics, its band structure reveals that the electrons behave as mass-less fermions with very high mobility, up to 200,000 $\text{cm}^2/\text{V}\cdot\text{sec}$. This incredible mobility paves the way to a host of applications ranging from high-performance transistors to low-loss interconnects. Current state of the art copper interconnects suffer from a dramatic increase in resistivity for line widths below 100 nm, as shown in Fig. 1. As a result, other materials, such as graphene, are being studied as a potential replacement for copper in future technology nodes.

Nanometer-scale graphene wires are often referred to as graphene nanoribbons or GNRs. The high carrier mobility of graphene would seem to make it an ideal replacement for copper in future integrated circuits. However, in practice GNRs suffer from relatively poor performance primarily caused by carrier scattering. Scattering is caused by a number of mechanisms such as impurities-induced scattering, substrate-dependent scattering and Line-edge roughness (LER). As shown in Fig. 2, carrier mobility falls significantly for GNR widths below 60 nm due to LER which occurs due to fabrication induced edge roughness.

Our research targets the minimization of LER in GNRs and the creation of high quality large area graphene for high-performance graphene-based electronics and interconnects. We focus on CMOS-compatible physical structures that diminish LER effects for transistors and interconnects. Our current research focuses on high mobility sub-50 nm unsuspended interconnects that could directly be integrated with CMOS processes or All-Graphene circuits.

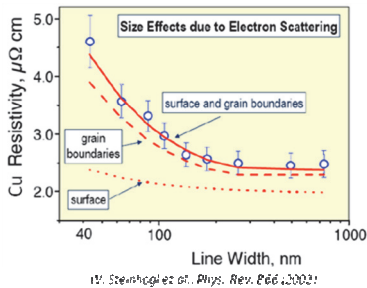


Fig. 1: Resistivity of Cu with scaling.

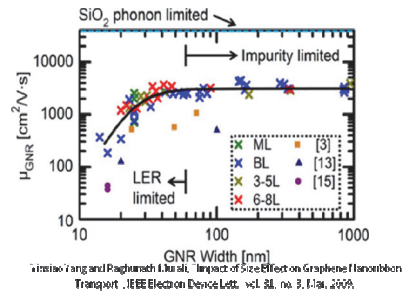


Fig 2: Mobility of GNR with GNR width for monolayer and multilayer Graphene.