

# Adaptive Multi-Antenna Receivers



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Multi-antenna transceivers employing antenna arrays improve the signal-to-noise-and-interference ratio (SINR) and are indispensable to combat the heavy signal attenuation at millimeter-wave frequencies. A simple multi-antenna receiver weights and combines the signals from several antenna elements. It thus acts as a spatial filter and enhances the signal coming from a particular direction while attenuating interferers coming from other directions. This selective gain, known as the array pattern may be steered by appropriately programming the weights. To take it one step further, this programming process can be automated so that the array adapts itself in response to a time-varying signal and interference field. Traditionally, adaptation is done digitally where all the antenna signals are digitized prior to multi-antenna processing. However, such an approach would require replicating the entire RF/analog front-end for every antenna to downconvert and digitize each antenna output; the power consumption and die area would be prohibitive with increasing number of antennas.

To alleviate this problem, the multi-antenna processing must be accomplished at RF or IF. Fig. 1 illustrates an IF-combined adaptive multi-antenna receiver architecture where complex weights are realized using vector combination of variable gain amplifiers. To further reduce the power consumption one can horizontally cascade single-transistor stages at a reduced supply voltage. In order to design stable, wideband, low-power array front-ends (47-67 GHz, < 15 mW per channel) this work explores different techniques both at local level (e.g. coupling multiple inductors within a gain stage) and at global level. A proof-of-concept 0.6V 4-antenna phased array receiver front-end incorporating these techniques has been fabricated in 45nm SOI CMOS.

