Low-Power, High-Radix, Crossbar Design For Networks-on-Chip

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Crossbar interconnects can offer high-radix, low-diameter networks for on-chip communication, but as the number of processors and caches on a single die increases, traditional crossbars scale poorly, exhibiting high energy consumption and high latency. As a solution to this scaling challenge, we propose low swing crossbar designs that decompose crossbars into efficient long interconnects that route the signals to/from the processors and caches and a compact crossbar switch core. We use capacitively driven wires for the long interconnect, since they offer low swing signaling, high bandwidths, and low energy consumption. For the switch, we further use capacitively coupled multiplexors that enable efficient high fan-in designs.

Capacitively coupled multiplexors connect each input to the output via a MOS capacitor. The selected input signal drives the output with a large “on” MOS capacitance, while the other inputs load the output with small “off” capacitances. This enables efficient high-radix multiplexors necessary for the crossbar core. Sense amplifiers are used to recover the low-swing outputs and to set the output DC bias via conductive coupling and feedback.

We designed a 16x16 low swing crossbar switch in a 40nm bulk CMOS process. The simulation results show 1.1x improvement for clock frequency and up to 4.3x improvement for energy consumption compared to a conventional multiplexor based crossbar. The next steps for our work will be fabricating a test chip, developing a design process for a crossbar, and building a CAD infrastructure for crossbar generation.

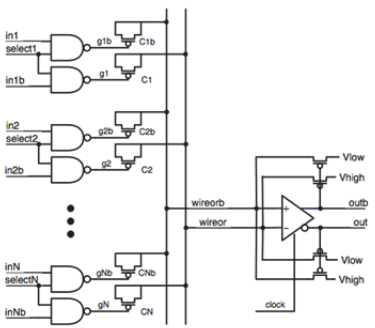

Fig. 1: Capacitively coupled multiplexor design

	Mux based crossbar	Low swing crossbar
Clock rate	2.2 GHz	2.5 GHz (1.1x)
Full BW energy consumption	1089 pJ	251 pJ (4.3x)
Half BW energy consumption	695 pJ	171 pJ (4x)
Min BW energy consumption	123 pJ	103 pJ (1.2x)

Fig 2: Proposed crossbar versus conventional design