Parasitic-Aware Common-Centroid FinFET Placement and Routing for Current-Ratio Matching

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The FinFET technology is regarded as a better alternative for modern high-performance and low-power integrated-circuit design due to more effective channel control and lower power consumption. However, the gate-misalignment problem resulting from process variation and the parasitic resistance resulting from interconnecting wires based on the FinFET technology becomes even more severe compared with the conventional planar CMOS technology. Such gate misalignment and unwanted parasitic resistance may increase the threshold voltage and decrease the drain current of transistors. When applying the FinFET technology to analog circuit design, the variation of drain currents can destroy current-ratio matching among transistors and degrade circuit performance. In this article, we present the first FinFET placement and routing algorithms for layout generation of a common-centroid FinFET array to precisely match the current ratios among transistors. Experimental results show that the proposed matching-driven FinFET placement and routing algorithms can obtain the best current-ratio matching compared with the state-of-the-art common-centroid placer.

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CCS Concepts: • **Hardware** → **Physical synthesis**; *Full-custom circuits;*

Additional Key Words and Phrases: Analog placement, routing, FinFET, gate misalignment, parasitic resistance, common centroid, current-ratio matching

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1. INTRODUCTION

In modern system-on-chip (SoC) design, the voltage of a transistor has been aggressively operated from the traditional super-threshold region to the sub/near-threshold region to effectively reduce power consumption of integrated circuits [Dreslinski et al.

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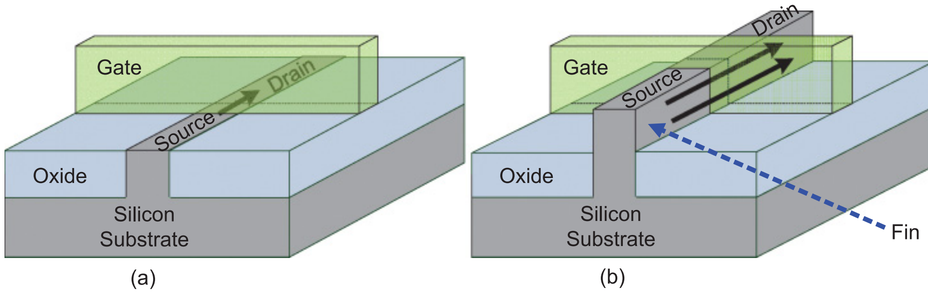

Fig. 1. Structural comparison between MOSFET and FinFET [Intel 2011]. (a) An example of planar MOSFET. (b) An example of 3-D FinFET.

2010]. When MOSFET operates in the on state, it forms a conductive channel in the silicon region under the gate electrode, as shown in Figure 1(a). As the conventional planar CMOS technology scales down to the 22*nm* node and beyond, the conductive channel becomes shorter and more challenging to effectively control short-channel effects (SCEs) [ITRS 2012]. Consequently, high-leakage current and threshold voltage variation will significantly affect the circuit performance, power dissipation, and reliability of circuits.

To overcome the difficulty of planar CMOS scaling, several new device technologies have been developed as alternatives to the bulk-silicon MOSFET structure for improved reliability. Among these device technologies, the three-dimensional (3-D) aspect of the Fin Field Effect Transistor (FinFET) has been regarded as one of the most promising technologies to substitute for the bulk-silicon MOSFET for ultimate scaling [Chiarella et al. 2010]. When the FinFET operates in the on state, it forms a conductive channel wrapped by a vertical silicon "fin," as in Figure 1(b). With the wraparound gate structure, FinFETs can better control the drain-source channel to alleviate SCEs and reduce random dopant fluctuations by near-intrinsic channel doping [Rasouli et al. 2009]; hence, both leakage current and threshold voltage variation can be significantly reduced [Chiarella et al. 2010]. With these advantages, it has been suggested to design the analog integrated circuits with FinFETs for greater improvement of power, performance, and chip area [Wambacq et al. 2007].

Although the FinFET technology can effectively minimize the impact from SCEs and benefit power, performance, and chip area of integrated circuits, some lithography-induced process variations and layout-induced parasitic effects become even more severe.

1.1. Current Mismatch Due to Gate Misalignment

Due to the gate misalignment, the position of the printed gate of a FinFET may deviate from the expected position after a set of lithography processes, which increases the threshold voltage and decreases the drain current of the FinFET [Valin et al. 2012; Fulde et al. 2007; Sarangia et al. 2013]. Figure 2 shows an example of gate misalignment. Ideally, the gate of a FinFET is expected to be located at the center between source and drain, as shown in Figure 2(a). However, the printed gate is usually misaligned due to process variation, as shown in Figure 2(b). According to Valin et al. [2012], the misaligned distance can be as large as 5*nm* either to the source side or the drain side for a 10*nm* process technology. Sarangia et al. [2013] reported that the threshold voltage of a FinFET, V_{th}, is more sensitive with source-side misalignment than with drain-side misalignment. In the worst case, when the gate is misaligned to the drain side of a FinFET by 5*nm*, V_{th} is increased by 0.01V. On the other hand, when

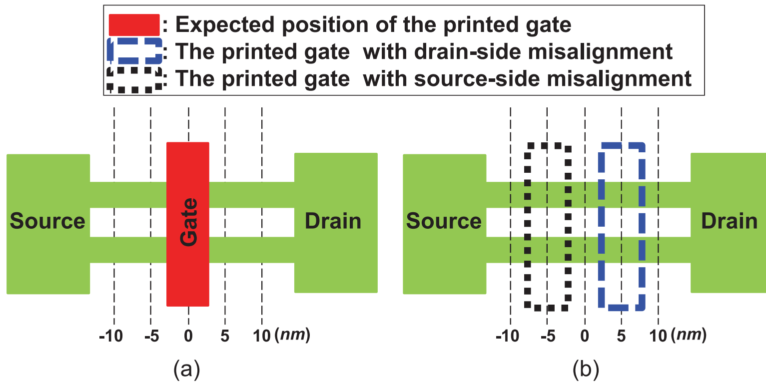

Fig. 2. An example of gate misalignment of a FinFET [Valin et al. 2012]. (a) An ideal FinFET without gate misalignment. (b) A real FinFET with either drain-side or source-side gate misalignment.

the gate is misaligned to the source side of a FinFET by $5nm$, V_{th} is increased by 0.05V. This increment can significantly degrade the drain current of the FinFET by 40% with a supply voltage of 1V.

As most of the analog building blocks, such as current mirrors and differential pairs, require highly matched drain current, any current variation due to gate misalignment may destroy current-ratio matching and degrade circuit performance. Consequently, it is essential to consider the existence of gate misalignment during the layout design of these building blocks. It should be noted that, during IC fabrication, the direction and distance of gate misalignment of different FinFETs on the same chip are usually the same. What designers need to do is to carefully arrange the orientations of all FinFETs within a current mirror or a differential pair such that the ratio of the drain current among different transistors in a current mirror or a differential pair can be perfectly matched [Fulde et al. 2007].

1.2. Current Mismatch Due to Parasitic Resistance

In addition to gate misalignment, based on the FinFET technology, the parasitic resistance of interconnecting wires becomes nonnegligible [Subramanian et al. 2006]. It gradually dominates the performance, signal integrity, and reliability of circuit designs [Baldi et al. 2001]. Without carefully considering parasitic resistance in analog IC layouts, the drain current of a transistor can be dramatically changed. As mentioned in Section 1.1, most of the analog building blocks, such as current mirrors and differential pairs, are very sensitive to the current variation or current mismatch; any current variation due to parasitic resistance can also destroy current-ratio matching and degrade circuit performance. Therefore, it is also necessary to consider the existence of routing-induced parasitic resistance during the layout design of these building blocks.

A current mirror with one reference transistor, t_{Ref}, and k scaled transistors, t_1, $t_2, \dots, t_k$, as shown in Figure 3(a), is to produce a set of constant replicated currents, I_1, $I_2, \dots, I_k$, flowing through $t_1, t_2, \dots, t_k$, regardless of its loading by copying the reference current, I_{Ref}, flowing through t_{Ref}. If the size, or the channel width, of a scaled transistor, t_i, is n times larger than that of t_{Ref}, I_i is scaled by a factor of n with respect to I_{Ref}. To reduce transistor mismatch due to process variation, each transistor is decomposed into several unit transistors, as shown in Figure 3(b). The unit transistors are then placed symmetrically with respect to a common center point, as shown in Figure 3(c).

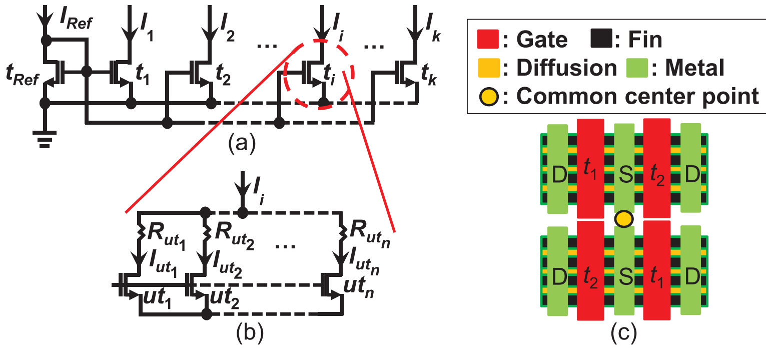

Fig. 3. (a) A current mirror with one reference transistor and k scaled transistors. (b) Transistor decomposition reducing the impact from process variation, but increasing parasitic resistance. (c) An example common-centroid FinFET placement of a current mirror with one reference transistor, t_1, and one scaled transistor, t_2, where t_1 and t_2 are decomposed into two unit transistors, respectively.

In Figure 3(a), as the source terminals of different transistors in a current mirror are fully connected, the routing wires connecting the source terminals of different transistors are short enough; hence, the respective parasitic resistance is negligible. However, when generating a layout of a great number of unit transistors with the common-centroid constraint, some unit transistors belonging to the same transistor, t_i, may be placed far away from each other. There exists a nonnegligible parasitic resistance, R_{ut_j}, corresponding to the routing wires connecting the drain terminal of a unit transistor, ut_j, and the drain terminals of other unit transistors, as shown in Figure 3(b). Consequently, it is essential to match the interconnecting wirelength during common-centroid FinFET placement and routing for better current-ratio matching such that the current mismatch due to the existence of parasitic resistance is reduced.

1.3. Previous Works

To generate a matched layout of the transistors in a current mirror or a differential pair, all the previous works [Ma et al. 2011; Lin et al. 2011; Xiao and Young 2009; Lin et al. 2009, 2007; Long et al. 2005; Ma et al. 2007; Yan et al. 2006; Zhang et al. 2010] presented various common-centroid placement and routing approaches for planar MOSFETs with the considerations of coincidence, symmetry, dispersion, and compactness [Hastings. 2006]. None of the previous works considered the impact of gate misalignment arising from the FinFET technology and the matching of parasitic resistance during common-centroid placement and routing. Although Long et al. [2005] mentioned the chirality condition of transistors within a common-centroid structure, this chirality condition cannot achieve the best current-ratio matching with the impact of gate misalignment.

Other recent works [Huang et al. 2013; Lin et al. 2012b; Ho et al. 2013; Li et al. 2014; Lin et al. 2012a, 2013, 2014] focused on the optimization of common-centroid capacitor placement and routing, but the capacitors in these works are still not associated with the FinFET technology and none considered the impact of parasitic resistance during common-centroid placement and routing.

As a result, a common-centroid layout having the best current-ratio matching with the existence of gate misalignment and parasitic resistance cannot be successfully generated by existing approaches.

1.4. Our Contributions

The contributions of this article are summarized as follows:

—We propose the *first* common-centroid FinFET placement and routing formulation that simultaneously considers the impact of gate misalignment and parasitic resistance, together with all conventional common-centroid rules, including coincidence, symmetry, dispersion, and compactness, for next-generation analog design.
—We derive a new quality metric to evaluate current-ratio matching among transistors in a current mirror with the existence of gate misalignment and parasitic resistance within a common-centroid FinFET array.
—Based on the derived quality metric and the spatial correlation model, we present novel parasitic-aware FinFET placement and routing algorithms to optimize current-ratio matching while maximizing the dispersion degree of a common-centroid FinFET array.
—Our experimental results show that the proposed approach can achieve much better current-ratio matching among transistors in a current mirror with the existence of gate misalignment and parasitic resistance while maintaining high dispersion degree.

The rest of this article is organized as follows: Section 2 reviews the spatial correlation model for evaluating the dispersion degree of a common-centroid FinFET placement. Section 3 demonstrates the current mismatch resulting from the impact of gate misalignment and parasitic resistance. Section 4 details the proposed common-centroid FinFET placement and routing algorithms. Section 5 contains the experimental results. We present our conclusions in Section 6.

2. EVALUATION OF DISPERSION DEGREE WITH SPATIAL CORRELATION MODEL

When generating the common-centroid placement of a current mirror, it is necessary to optimize the matching quality among the reference transistor and all the other scaled transistors for accurate scaling factors. According to Lin et al. [2012b], the transistor mismatch occurring due to process variation can be divided into two categories: systematic mismatch and random mismatch. To reduce systematic mismatch, each transistor is decomposed into several unit transistors that are placed symmetrically with respect to a common center point, as shown in Figure 3(c). On the other hand, random mismatch is mainly related to statistical fluctuations in processing conditions or material properties. As these fluctuations are in random mechanisms, all unit transistors of each transistor should be evenly distributed throughout a common-centroid placement to exhibit the highest degree of dispersion [Razavi 2000].

Luo et al. [2008] proposed a spatial correlation model to measure the overall correlation coefficient, or the dispersion degree, ρ, of a common-centroid placement. For n transistors, ρ equals the summation of all correlation coefficients of a pair of transistors, which is defined in Equation (1).

$$\rho = \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} \sigma_{ij}, \tag{1}$$

where σ_{ij} is the correlation coefficient of two transistors, t_i and t_j. By assuming that t_i consists of n_i unit transistors and t_j consists of n_j unit transistors, σ_{ij} can be calculated based on Equation (2).

$$\sigma_{ij} = \frac{\sum_{a=1}^{n_i} \sum_{b=1}^{n_j} \rho_{ab}}{\sqrt{X_i \times X_j}}, \tag{2}$$

where ρ_{ab} is the correlation coefficient of two unit transistors, and $X_k = n_k + 2 \times \sum_{a=1}^{n_k-1} \sum_{b=a+1}^{n_k} \rho_{ab}$. Assume that a set of unit transistors of all transistors are arranged in a matrix with N_r rows and N_c columns. Given two unit transistors, ut_i and ut_j,

located at the entries in the r_i^{th} row and c_i^{th} column and the r_j^{th} row and c_j^{th} column, respectively, their correlation coefficient, ρ_{ij}, is defined in Equation (3).

$$\rho_{ij} = \rho_u^{\sqrt{(r_i - r_j)^2 \times l_r^2 + (c_i - c_j)^2 \times l_c^2}}, \quad (3)$$

where $0 < \rho_u < 1$, and l_r (l_c) is the center-to-center distance between vertically (horizontally) adjacent transistors.

Based on the correlation model, the larger the ρ, the better dispersion degree of a common-centroid placement.

3. CURRENT MISMATCH RESULTING FROM GATE MISALIGNMENT AND PARASITIC RESISTANCE

As mentioned in Section 1, the issues of gate misalignment and parasitic resistance based on the FinFET technology may have high impact on the drain currents of different transistors in a current mirror. In addition to evaluating the dispersion degree of a common-centroid placement based on the spatial correlation model, it is also necessary to study how to evaluate the matching quality of drain currents with the existence of gate misalignment and parasitic resistance.

In Section 3.1, we first derive the quality metric for evaluating the current mismatch of a current mirror within a common-centroid FinFET array with the existence of gate misalignment and parasitic resistance. In Section 3.2, we present a case study to show the importance of determining the orientation of each transistor and considering the matching of parasitic resistance during common-centroid FinFET placement and routing for minimizing the impact of gate misalignment and parasitic resistance.

3.1. Evaluation of Current Mismatch

To copy the reference current to other scaled transistors, the scaled transistor must be operated in the saturation region [Razavi 2000]. According to Subramanian et al. [2006], the drain current of a unit transistor, ut_i, in the saturation region with the existence of parasitic resistance at the drain terminal is defined by Equation (4).

$$I_{ut_i} = \frac{\frac{\mu \times C_{ox} \times W_{ut}}{2 \times L_{ut}} \times (V_{GS} - V_{th})^2}{1 + \frac{\mu \times C_{ox} \times W_{ut}}{L_{ut}} \times (V_{GS} - V_{th}) \times R_{ut_i}} = \frac{f_1(V_{th})}{1 + f_2(V_{th}) \times R_{ut_i}}, \quad (4)$$

where R_{ut_i} represents the parasitic resistance corresponding to the wires connecting the drain terminal of ut_i and the drain terminal of other unit transistors belonging to the same transistor. We adopt the 10*nm* FinFET technology with 1V supply voltage. The process parameters, as listed in Table I, can be obtained from ITRS [2012] and Liu et al. [1998].

As the impact of gate misalignment may increase V_{th} of transistors, I_{ut_i} can be written as functions of V_{th}. With the consideration of gate misalignment, the threshold voltage of the unit transistors with drain-side misalignment is denoted as V_{th}^d and the threshold voltage of the unit transistors with source-side misalignment is denoted as V_{th}^s. Based on Equation (4), if a transistor, t_i, containing n^d unit transistors with drain-side gate misalignment and n^s unit transistors with source-side misalignment, where $n = n^d + n^s$, the drain current, I_i, with the existence of gate misalignment and parasitic resistance

Table I. Parameters of the 10*nm* FinFET Process Technology
[ITRS 2012; Liu et al. 1998]

Parameter	Value	Description
μ	$0.03\,\frac{m}{V\cdot s}$	Carrier mobility
C_{ox}	3.453E-02 $\frac{F}{m^2}$	Capacitance of gate oxide
L_{ut} (W_{ut})	30*nm* (75*nm*)	Channel length (width) of a unit transistor
V_{GS}	1V	Voltage difference between gate and source terminals
V_{th}	0.15V	Threshold voltage
V_{th}^d (V_{th}^s)	0.151V (0.155V)	Threshold voltage with drain-side (source-side) misalignment
R_s	$0.07\,\frac{\Omega}{nm}$	Sheet resistance

can be expressed by Equation (5).

$$\begin{aligned} I_i &= I^d_{ut_1} + \cdots + I^d_{ut_j} + I^s_{ut_{j+1}} + \cdots + I^s_{ut_n} \\ &= \left(\frac{1}{1 + f_2(V^d_{th}) \times R_{ut_1}} + \cdots + \frac{1}{1 + f_2(V^d_{th}) \times R_{ut_j}} \right) \times f_1(V^d_{th}) \\ &\quad + \left(\frac{1}{1 + f_2(V^s_{th}) \times R_{ut_{j+1}}} + \cdots + \frac{1}{1 + f_2(V^s_{th}) \times R_{ut_n}} \right) \times f_1(V^s_{th}), \end{aligned} \tag{5}$$

where V^d_{th} (V^s_{th}) denotes the respective threshold voltage of ut_i with the drain (source)-side misalignment, and $I^d_{ut_i}$ ($I^s_{ut_i}$) is the resulting drain current of ut_i with V^d_{th} (V^s_{th}).

We apply Taylor series expansion to Equation (5) since all parameters, including μ, C_{ox}, and $\frac{W_{ut}}{L_{ut}}$, in the function, f_2, are small constants based on Table I, and R_{ut_i} is also less than 1 Ω. Consequently, we have the following approximations: $\frac{1}{1+f_2(V^d_{th})\times R_{ut_i}} \approx 1 - f_2(V^d_{th}) \times R_{ut_i}$, and $\frac{1}{1+f_2(V^s_{th})\times R_{ut_i}}$ can be approximated similarly. As a result, I_i can be transformed into Equation (6).

$$\begin{aligned} I_i &= \left(n^d - f_2(V^d_{th}) \times (R_{ut_1} + \cdots + R_{ut_j})\right) \times f_1(V^d_{th}) \\ &\quad + \left(n^s - f_2(V^s_{th}) \times (R_{ut_{j+1}} + \cdots + R_{ut_n})\right) \times f_1(V^s_{th}) \\ &= \left(n^d - f_2(V^d_{th}) \times R^d_i\right) \times f_1(V^d_{th}) + \left(n^s - f_2(V^s_{th}) \times R^s_i\right) \times f_1(V^s_{th}), \end{aligned} \tag{6}$$

where R^d_i (R^s_i) $= L^d_i$ (L^s_i)$\times R_s$. L^d_i (L^s_i) is total wirelength of the interconnection among the drain (source) terminals of ut_i and those of other unit transistors, and R^d_i (R^s_i) is the parasitic resistance corresponding to L^d_i (L^s_i).

Based on Equation (6) and the current mirror, as seen in Figure 3, we want to optimize the current-ratio matching among different transistors in the current mirror. The objective of optimizing current-ratio matching is shown in Equation (7).

$$\begin{aligned} & I_1 : I_2 : \cdots : I_k = n_1 : n_2 : \cdots : n_k \\ & = \left(n^d_1 - f_2(V^d_{th}) \times R^d_1\right) \times f_1(V^d_{th}) + \left(n^s_1 - f_2(V^s_{th}) \times R^s_1\right) \times f_1(V^s_{th}) \\ & \quad : \left(n^d_2 - f_2(V^d_{th}) \times R^d_2\right) \times f_1(V^d_{th}) + \left(n^s_2 - f_2(V^s_{th}) \times R^s_2\right) \times f_1(V^s_{th}) \\ & \quad : \cdots : \left(n^d_k - f_2(V^d_{th}) \times R^d_k\right) \times f_1(V^d_{th}) + \left(n^s_k - f_2(V^s_{th}) \times R^s_k\right) \times f_1(V^s_{th}) \end{aligned}. \tag{7}$$

By applying the multiplication property and substituting n_i with $n_i^d + n_i^s$, we can obtain Equations (8) and (9), respectively,

$$\begin{aligned}&\frac{1}{n_i} \times \left(\left(n_i^d - f_2\left(V_{th}^d\right) \times R_i^d\right) \times f_1\left(V_{th}^d\right) + \left(n_i^s - f_2\left(V_{th}^s\right) \times R_i^s\right) \times f_1\left(V_{th}^s\right)\right)\\ &\quad = \frac{1}{n_j} \times \left(\left(n_j^d - f_2\left(V_{th}^d\right) \times R_j^d\right) \times f_1\left(V_{th}^d\right) + \left(n_j^s - f_2\left(V_{th}^s\right) \times R_j^s\right) \times f_1\left(V_{th}^s\right)\right),\\ &\quad \forall i, j, 1 \le i \le k-1, 2 \le j \le k.\end{aligned} \tag{8}$$

$$\begin{aligned}\epsilon_{i-j} = \epsilon_{i-j}^G + \epsilon_{i-j}^P = &\frac{\alpha \times \left(n_i^d \times n_j^s - n_j^d \times n_i^s\right)}{n_i \times n_j}\\ &+ \left(\frac{\beta \times \left(R_j^d \times n_i - R_i^d \times n_j\right)}{n_i \times n_j} + \frac{\gamma \times \left(R_j^s \times n_i - R_i^s \times n_j\right)}{n_i \times n_j}\right),\\ &\forall i, j, 1 \le i \le k-1, 2 \le j \le k.\end{aligned} \tag{9}$$

In Equation (9), ϵ_{i-j} denotes the current mismatch between t_i and t_j, and ϵ_{i-j}^G (ϵ_{i-j}^P) is the current mismatch resulting from the impact of gate misalignment (parasitic resistance). $\alpha = f_1(V_{th}^d) - f_1(V_{th}^s)$, $\beta = f_1(V_{th}^d) \times f_2(V_{th}^d)$, and $\gamma = f_1(V_{th}^s) \times f_2(V_{th}^s)$. If the resulting current ratio equals the expected current ratio (i.e., no current mismatch), ϵ_{i-j} equals 0. Consequently, the overall current mismatch among different transistors in a current mirror is obtained by summing up all ϵ_{i-j}, as seen in Equation (10).

$$\begin{aligned}\epsilon &= \epsilon^G + \epsilon^P\\ &= \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \frac{\left(f_1\left(V_{th}^d\right) - f_1\left(V_{th}^s\right)\right) \times \left(n_i^d \times n_j^s - n_j^d \times n_i^s\right)}{n_i \times n_j}\\ &\quad + \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \left(\frac{f_1\left(V_{th}^d\right) \times f_2\left(V_{th}^d\right) \times \left(R_j^d \times n_i - R_i^d \times n_j\right)}{n_i \times n_j}\right.\\ &\quad \left. + \frac{f_1\left(V_{th}^s\right) \times f_2\left(V_{th}^s\right) \times \left(R_j^s \times n_i - R_i^s \times n_j\right)}{n_i \times n_j}\right).\end{aligned} \tag{10}$$

3.2. A Case Study

We conduct a case study, as demonstrated in Figure 4, for the following purposes: (1) comparing different common-centroid arrays with and without considering gate misalignment and parasitic resistance, (2) evaluating the resulting current mismatch and dispersion degree of each common-centroid array, and (3) justifying the correctness of Equation (10) based on the drain current model in Equation (4).

The current mirror in Figure 4(a) consists of one reference transistor and three scaled transistors. The reference current, I_{Ref}, flows through the reference transistor, t_{Ref}, and the replicated currents, I_1, I_2, and I_3, are copied from I_{Ref} to other scaled transistors, t_1, t_2, and t_3 with different scaling factors. The scaling factors, or the number of unit transistors of t_{Ref}, t_1, t_2, and t_3, are 2, 2, 4, and 8, respectively; thus, the expected current ratio, $I_{Ref} : I_1 : I_2 : I_3$, is $1:1:2:4$. Figures 4(b)–(d) give three different common-centroid FinFET layouts of Figure 4(a) without and with considering gate misalignment and parasitic resistance, in which the indices of the unit transistors of t_{Ref}, t_1, t_2, and t_3 are represented by 1, 2, 3, and 4, respectively.

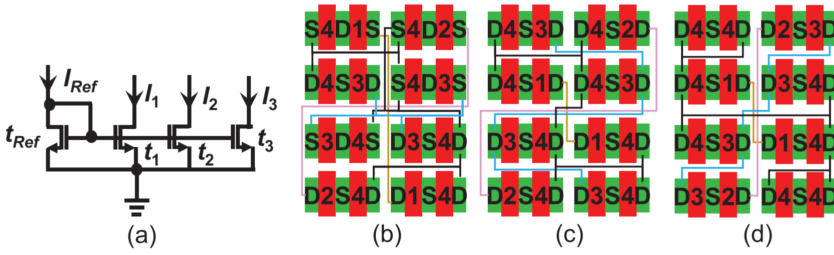

Fig. 4. Comparisons of different common-centroid FinFET arrays. (a) A current mirror with the ideal current ratio, $I_{Ref} : I_1 : I_2 : I_3 = 1 : 1 : 2 : 4$. (b) The FinFET placement and routing without considering gate misalignment and parasitic resistance. (c) The FinFET placement and routing considering only gate misalignment. (d) The FinFET placement and routing considering both gate misalignment and parasitic resistance.

Table II. Comparisons of the Simulated Current Ratios, Current Mismatch (ϵ^G and ϵ^P), and Dispersion Degree (ρ) for the Resulting Common-Centroid Layouts in Figures 4(b)–(d)

Cases	Simulated current ratio	ϵ^G	ϵ^P	ρ
Figure 4(b)	$1 : 0.9971 : 2.2044 : 4.3048$ $L_1^s : L_2^s : L_3^s : L_4^s = 4 : 6 : 0 : 4$ $L_1^d : L_2^d : L_3^d : L_4^d = 0 : 0 : 8 : 13$	0.192	0.004	5.733
Figure 4(c)	$1 : 0.994 : 1.994 : 3.997$ $L_1^s : L_2^s : L_3^s : L_4^s = 1 : 3 : 4 : 5$ $L_1^d : L_2^d : L_3^d : L_4^d = 1 : 3 : 4 : 5$	0.000	0.010	5.749
Figure 4(d)	$1 : 0.997 : 1.997 : 3.997$ $L_1^s : L_2^s : L_3^s : L_4^s = 1 : 2 : 3 : 5$ $L_1^d : L_2^d : L_3^d : L_4^d = 1 : 2 : 3 : 5$	0.000	0.004	5.762

For each common-centroid layout in Figure 4, we evaluate the dispersion degree and current mismatch based on Equations (1) and (10), and calculate the resulting drain current of each transistor with the consideration of parasitic resistance based on Equation (4). Without loss of generality, we assume that the printed gates of all unit transistors in each common-centroid placement are misaligned to the right side, which is also the worst-case process variation; thus, the printed gate of a unit transistor has either drain-side or source-side misalignment according to its orientation. As mentioned in Section 1.1, in the worst case, V_{th} is increased by 0.01V (0.05V) with drain-side (source-side) misalignment based on a 10*nm* FinFET technology with 1V supply voltage. We also adopt these settings to adjust the threshold voltage of each unit transistor when calculating the drain current of each transistor.

Table II reports the simulated current ratio, current mismatch (ϵ^G and ϵ^P), and dispersion degree (ρ) for all common-centroid layouts in Figures 4(b)–(d). According to the Table II, the common-centroid layout in Figure 4(b) without considering both gate misalignment and parasitic resistance results in the worst current mismatch, $\epsilon(= \epsilon^G + \epsilon^P)$. The common-centroid layout in Figure 4(c), with the only consideration of gate misalignment and without considering the impact of parasitic resistance, results in the best ϵ^G, but the worst ϵ^P. With the consideration of both gate misalignment and parasitic resistance, the common-centroid layout in Figure 4(d) achieves the best ϵ^G and ϵ^P, thus the best current-ratio matching. Consequently, it is very important to consider both gate misalignment and parasitic resistance when designing the layout of a common-centroid FinFET array.

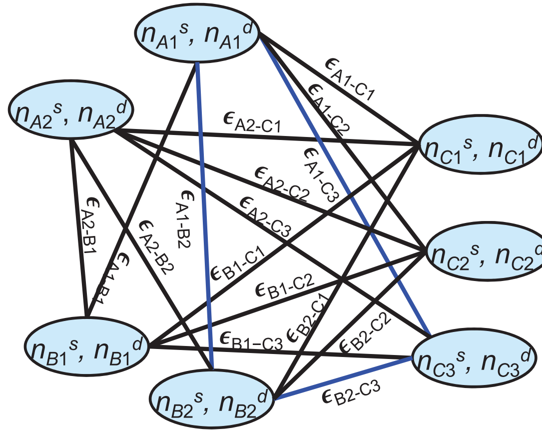

Fig. 5. An example minimum-weight-clique formulation for a current mirror with three transistors, A, B, and C. Each transistor has 2, 2, and 3 possible configurations of unit transistors' orientations, respectively.

4. COMMON-CENTROID FINFET PLACEMENT AND ROUTING ALGORITHMS

Based on the evaluation metrics of dispersion degree and current mismatch in Equations (1) and (10), we propose the generation of an optimized common-centroid FinFET layout considering the impact of gate misalignment and parasitic resistance while maximizing the dispersion degree. Our approach starts with the determination of unit transistors' orientations while minimizing the current mismatch resulting from the gate misalignment (Section 4.1). Based on the determined unit transistors' orientations, we then generate an initial common-centroid FinFET placement by maximizing diffusion sharing and dispersion degree among unit transistors in the same row while restricting the placement range (Section 4.2) such that the current mismatch due to the impact of parasitic resistance is reduced. Once the placement of each row is obtained, we further refine the placement by maximizing the dispersion degree among unit transistors in different rows (Section 4.3). Finally, we perform parasitic-aware routing to generate the routing topology of each net while improving the current-ratio matching among different transistors (Section 4.4).

4.1. Determination of Unit Transistor Orientations

In order to reduce the current mismatch due to gate misalignment, the unit transistors' orientations must be properly determined. We formulate the problem as finding the minimum-weight clique [Cormen et al. 2001] in an undirected graph to simultaneously determine the unit transistors' orientations. Each vertex in the graph represents one configuration of the unit transistors' orientations of a transistor, t_i, which has n_i^s unit transistors with source-side misalignment and n_i^d unit transistors with drain-side misalignment, respectively. There exists an edge between two vertices if the vertices correspond to two different transistors, t_i and t_j. The edge weight, ϵ_{i-j}^G, which can be calculated by Equation (9), denotes the current mismatch between t_i and t_j based on the configurations of unit transistors' orientations represented by the vertices.

Solving the minimum-weight-clique problem in a graph is known as an NP-complete problem. We apply the heuristic [Östergård 2001] using the branch-and-bound algorithm. We enumerate all possible configurations (i.e., a k-finger FinFET has k+1 configurations whose orientations are the combination of source-side misalignment and drain-side misalignment) of unit transistor orientations for each transistor in the graph. Figure 5 shows a minimum-weight-clique formulation for a current mirror with

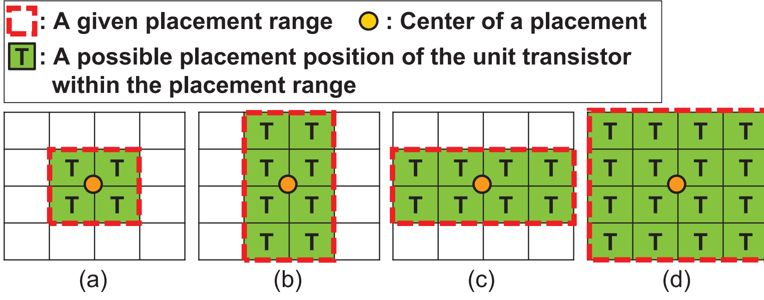

Fig. 6. A set of four probable placement range constraints within a 4×4 array for placing the unit transistors of t_i. (a) $\{D^i_C, D^i_R\} = \{1, 1\}$. (b) $\{D^i_C, D^i_R\} = \{1, 2\}$. (c) $\{D^i_C, D^i_R\} = \{2, 1\}$. (d) $\{D^i_C, D^i_R\} = \{2, 2\}$.

three transistors, A, B, and C, in which each transistor has 2, 2, and 3 possible configurations of unit transistors' orientations, respectively. By finding the minimum-weight clique in the undirected graph, the best configuration of unit transistors' orientations for each transistor can be determined such that the minimum current mismatch due to gate misalignment, ϵ^G, can be achieved.

4.2. Common-Centroid FinFET Placement Algorithm Considering Parasitic Resistance and Dispersion

Given the determined unit transistors' orientations, we want to generate an N_r-row and N_c-column common-centroid FinFET placement while maintaining unit transistors' orientations, minimizing current mismatch due to parasitic resistance, and maximizing the dispersion degree. Since the orientations of all unit transistors have been determined, the current mismatch of a common-centroid FinFET array is thus dominated by ϵ^P. We need to find an optimal placement leading to matched parasitic resistance after routing.

To achieve this goal, we introduce a placement range constraint for each transistor to restrict the placement region of the corresponding unit transistors within an allowable distance, which is defined in the following:

Definition 1. The **placement range constraint** for a transistor, t_i, is a 2-tuple combination, denoted by $\{D^i_C, D^i_R\}$, which restricts the location of a unit transistor of t_i within the distance of D^i_C (D^i_R) in x-direction (y-direction) from the center of an N_r-row and N_c-column unit transistor array.

We determine $\{D^i_C, D^i_R\}$ of each transistor, t_i, in a current mirror by minimizing the current mismatch $\epsilon_{(i)-(j)}$ between any two transistors, t_i and t_j. For a transistor, t_i, we first create a placement region with the range from the $(\lceil\frac{(N_c+1)}{2} - D^i_C\rceil)^{th}$ column to the $(\lfloor\frac{(N_c+1)}{2} + D^i_C\rfloor)^{th}$ column and from the $(\lceil\frac{(N_r+1)}{2} - D^i_R\rceil)^{th}$ row to the $(\lfloor\frac{(N_r+1)}{2} + D^i_R\rfloor)^{th}$ row, respectively. By iteratively enumerating all possible combinations of $\{D^i_C, D^i_R\}$, where $1 \le D^i_C \le \frac{N_c}{2}$ and $1 \le D^i_R \le \frac{N_r}{2}$, a set of probable placement range constraints, $\{1, 1\}, \ldots,$ $\{1, \lfloor\frac{(N_r)}{2}\rfloor\}, \{2, 1\}, \ldots, \{\lfloor\frac{(N_c)}{2}\rfloor, \lfloor\frac{(N_r)}{2}\rfloor\}$, can be derived.

Figure 6 gives an example of four probable placement range constraints within a 4×4 array for placing the unit transistors of t_i. By connecting the unit transistors of the reference transistor, t_{Ref}, with the minimum wirelength, we can optimize the wirelength of the scaled transistors, t_i, to maximize the matching of parasitic resistance between t_{Ref} and t_i. For each derived $\{D^i_C, D^i_R\}$, we estimate the resulting wirelength of a net connecting all drain terminals of the unit transistors of t_i within the possible placement region. Based on the estimated wirelength and Equation (11), which is

derived from Equation (9), we can obtain the current mismatch between t_i and t_{Ref}. We finally choose the best placement range constraint for t_i, resulting in the minimum current mismatch according to Equation (11).

$$\epsilon_{(Ref)-(i)} = \frac{\left(f_1(V_{th}^d) - f_1(V_{th}^s)\right) \times \left(n_{Ref}^d \times n_i^s - n_i^d \times n_{Ref}^s\right)}{n_{Ref} \times n_i} + \frac{f_1(V_{th}^d) \times f_2(V_{th}^d) \times \left(R_i^d \times n_{Ref} - R_{Ref}^d \times n_i\right)}{n_{Ref} \times n_i} + \frac{f_1(V_{th}^s) \times f_2(V_{th}^s) \times \left(R_i^s \times n_{Ref} - R_{Ref}^s \times n_i\right)}{n_{Ref} \times n_i}. \quad (11)$$

Once the placement range constraints of all transistors are obtained, we then perform common-centroid placement according to the optimized placement range constraints. The procedure of our placement algorithm consists of three major steps:

4.2.1. Row Assignment. Given a set of n_i unit transistors of a transistor, t_i, based on its placement range constraint, we evenly distribute $\frac{n_i}{2\times(\lceil\frac{(N_r)}{2}\rceil - \lceil\frac{(N_r+1)}{2} - D_R^i\rceil + 1)}$ unit transistors into each row between $(\lceil\frac{(N_r+1)}{2} - D_R^i\rceil)^{th}$ and $\lceil\frac{(N_r)}{2}\rceil^{th}$ such that the dispersion degree of a common-centroid FinFET placement can be maximized in the subsequent steps. If $\frac{n_i}{2} < (\lceil\frac{(N_r)}{2}\rceil - \lceil\frac{(N_r+1)}{2} - D_R^i\rceil + 1)$, we randomly assign the unit transistors into the rows between $(\lceil\frac{(N_r+1)}{2} - D_R^i\rceil)^{th}$ and $\lceil\frac{(N_r)}{2}\rceil^{th}$. During the row assignment, the placement range constraints of each transistor should also be considered.

4.2.2. Detailed Placement. Once all unit transistors are assigned to different rows, we generate the detailed placement of each row by searching Euler paths, while maximizing the dispersion and diffusion sharing [Naiknaware and Fiez 1999]. We construct the diffusion graph of the subcircuit in each row; then, we find the Euler paths on the diffusion graph [Naiknaware and Fiez 1999]. However, the diffusion graph that we used in this article is different from Naiknaware and Fiez [1999]. As described in Section 4.1, we have determined the unit transistors' orientations. To avoid degrading the current mismatch, the unit transistors' orientations cannot be changed during the search of the Euler path. Therefore, the constructed diffusion graph is a directed graph instead of an undirected graph used in Naiknaware and Fiez [1999], in which the number of directed edges originating from source node (S) to drain node (D) equals the number of unit transistors with drain-side misalignment, and vice versa.

According to the spatial correlation model in Section 2, to effectively maximize the dispersion degree of a common-centroid FinFET placement, all unit transistors belonging to the same transistor should be properly separated while the unit transistors belonging to different transistors should be as close as possible. For clear presentation, we define different kinds of unit transistors in Definition 2.

Definition 2. Two unit transistors are called **unrelated transistors** (**related transistors**), if they belong to different transistors, t_i and t_j (the same transistor, t_i).

To effectively maximize the dispersion degree of a common-centroid FinFET placement, we set a maximum separation (minimum separation) constraint, as defined in Definition 3, for two unrelated transistors (related transistors) to constrain the selection of edge during finding the Euler paths such that the dispersion degree can be effectively maximized.

Definition 3. A **maximum separation constraint** (**minimum separation constraint**) is the maximum (minimum) allowable distance between two neighboring

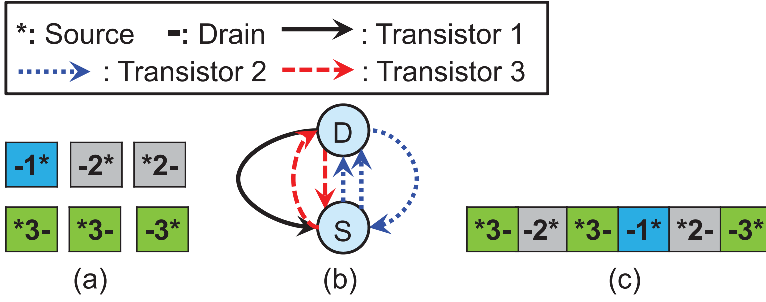

Fig. 7. An example of constructing the diffusion graph. (a) A set of unit transistors with fixed orientation. (b) The corresponding diffusion graph of (a). (c) The generated row placement by searching the diffusion graph in (b).

unrelated transistors (related transistors) when finding the Euler paths, which is denoted by D_{max_sep} (D_{min_sep}). The distance between two neighboring unit transistors refers to the number of unit transistors between the neighboring unit transistors.

During searching the Euler path, we choose only the edge satisfying both maximum and minimum separation constraints to properly distribute different unit transistors while maximizing the dispersion degree. To obtain a row placement leading to matched parasitic resistance after routing, we shall additionally verify the placement range constraint of each unit transistor during searching the corresponding Euler paths. Initially, D_{min_sep} is set to 0 and D_{max_sep} is set to the number of unit transistors in the row to start the procedure of searching the Euler paths. By iteratively increasing D_{min_sep} and decreasing D_{max_sep} during the procedure of searching the Euler path until an extra diffusion gap is required, the dispersion degree of the resulting row placement can be effectively maximized. After obtaining the Euler paths, the unit transistors on the same Euler path are merged with diffusion sharing.

Given a set of unit transistors with fixed orientation, as shown in Figure 7(a), a directed diffusion graph can be created, as given in Figure 7(b). Then, starting from the source node, as seen in Figure 7(b), an optimized row placement, as shown in Figure 7(c), can be obtained by iteratively searching the Euler paths with decreasing the maximum separation constraint and increasing the minimum separation constraint. In this example, the iteration stops when $D_{max_sep} = 3$ and $D_{min_sep} = 1$, which does not incur an extra diffusion gap. Moreover, for simplification, we assume that the source terminals/drain terminals of different unit transistors can be merged. If the source terminals/drain terminals of some unit transistors cannot be merged, extra diffusion gaps are created and multiple Euler paths will be obtained.

4.2.3. Symmetric Placement Generation. After obtaining the detailed placement of the first half of the rows with diffusion merging, we then generate the symmetric detailed placement of the second half of the rows in a reverse order. For the $(N_r - i + 1)^{th}$ row in the second half of the rows, the unit transistors are reversely placed according to the ith row in the first half of the rows. Figure 8 demonstrates the procedure of the overall common-centroid FinFET placement flow.

4.3. Dispersion Degree Maximization Considering Parasitic Resistance

After obtaining the initial common-centroid FinFET placement with optimized diffusion sharing and dispersion degree of the unit transistors in each row, we further maximize the dispersion degree of unit transistors in different rows by adjusting the relative positions of different unit transistors among different rows. We perform

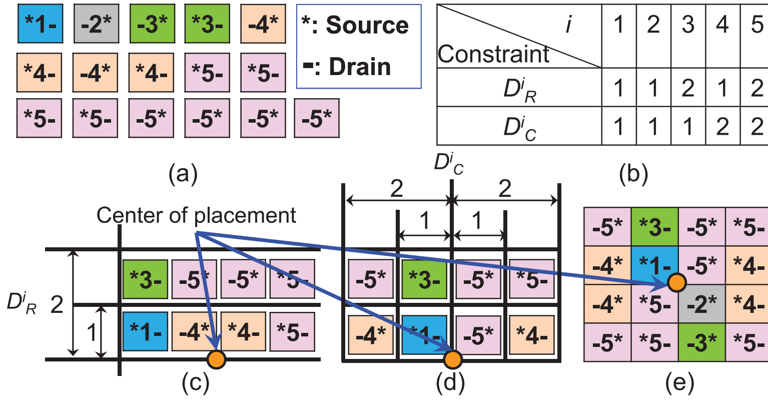

Fig. 8. An example of generating common-centroid FinFET placement with the consideration of parasitic resistance and dispersion. (a) A set of unit transistors with optimized orientations. (b) The placement range constraints of all transistors. (c) Row assignment of unit transistors, which maximizes dispersion degree and satisfies placement range constraints. (d) Detailed unit transistor placement, which maximizes diffusion sharing, optimizes minimum/maximum separation constraints, and satisfies placement range constraints. (e) Complete common-centroid FinFET placement.

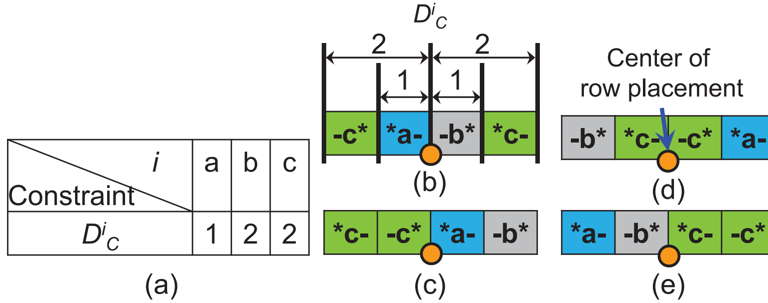

Fig. 9. An example of placement rotation in a row. (a) A set of given placement range constraints. (b) An initial row placement. (c)–(e) Three derived row placements after placement rotation. Only the placement in (c) satisfies the placement range constraints in (a).

placement rotation for each row by iteratively moving the unit transistor at the end of the row to the beginning of the row. During placement rotation, only the rotated placements satisfying the placement range constraints are reserved.

Figure 9 gives an example of placement rotation. The placement range constraints and the initial placement of a row are given in Figures 9(a) and 9(b), respectively. By iteratively moving the unit transistor at the end of the row to the beginning of the row, we can derive three different placements of the row, as shown in Figures 9(c)–(e), respectively. The placements in Figures 9(d) and 9(e) violate the placement distance constraint, $D^a_C = 1$, because the distance from the location of the unit transistor, a, to the center of the row is 2. Only the derived placement in Figure 9(c) is reserved. It should be noted that the placement rotation changes only the column position of the unit transistors; thus, we need to verify only D^i_C for each unit transistor, ut_i.

By performing the placement rotation for each row, a set of row placements satisfying placement range constraints can be derived. We then simultaneously select the best placements of all m rows with the largest dispersion degree of the unit transistors among different rows by applying the shortest path algorithm such that the optimal

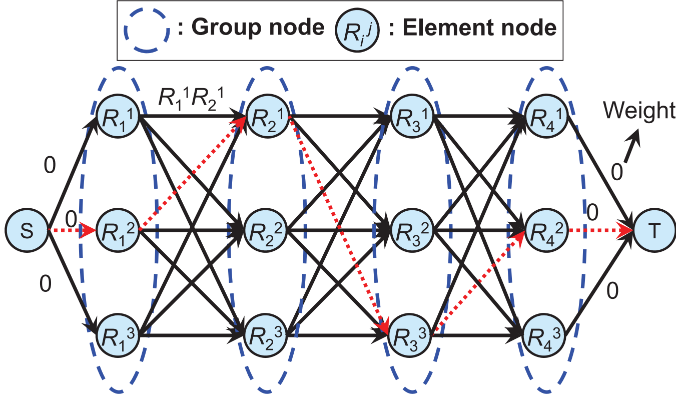

Fig. 10. An example of the shortest-path (SP) formulation for a 4-row common-centroid FinFET placement.

common-centroid FinFET placement with the consideration of gate misalignment, parasitic resistance, and dispersion degree can be obtained.

The simultaneous selection of the best placement of different rows is formulated as the shortest-path (SP) problem. Initially, a source node (S) and a sink node (T) are created, respectively. For a respective row, a group node is created, in which a set of element nodes representing the possible row placements are contained in the group node. Once the group nodes and element nodes are created, we then add a set of directed edges from S to each element node in the group node corresponding to the first row, and a set of directed edges from each element node in the group node corresponding to the last row to T, for whichn the weight of these edges are all zero. For two adjacent rows, there is a directed edge from an element node in the group node corresponding to the ith row to an element node in the group node corresponding to the $(i+1)^{th}$ row, where $1 \leq i < m$. The weight of each edge is calculated based on Equation (1), which indicates the dispersion degree. By finding the SP from S to T, the best placement of each row can be determined and the dispersion degree of the whole common-centroid FinFET placement can be further maximized.

Figure 10 shows an example of the SP formulation for a 4-row common-centroid FinFET placement. Each row has three possible row placements after placement rotation. After solving the SP problem, the 2nd, 1st, 3rd, and 2nd placements of the 1st, 2nd, 3rd, and 4th rows are selected to achieve the best common-centroid FinFET placement with the maximum dispersion degree.

4.4. Parasitic-Aware Routing

Once the optimized common-centroid FinFET placement is obtained, we perform parasitic-aware routing to connect the drain terminals of the unit transistors of each transistor while optimizing the routing wirelength to maximize the matching of parasitic resistance.

We first connect the unit transistors of the reference transistor, t_{Ref}, with the minimum wirelength. To connect the unit transistors of a scaled transistor, t_i, while maximizing the matching of parasitic resistance between t_{Ref} and t_i, we construct a complete graph for the unit transistors of t_i and find the minimum spanning tree (MST) [Cormen et al. 2001], where the weights of the edges are calculated by half-perimeter wirelength. By choosing the edges based on the nondecreasing order of the routing wirelength, we iteratively exchange the edges contained in the complete graph but not in the MST with the edges contained in the MST to further adjust the routing topology to

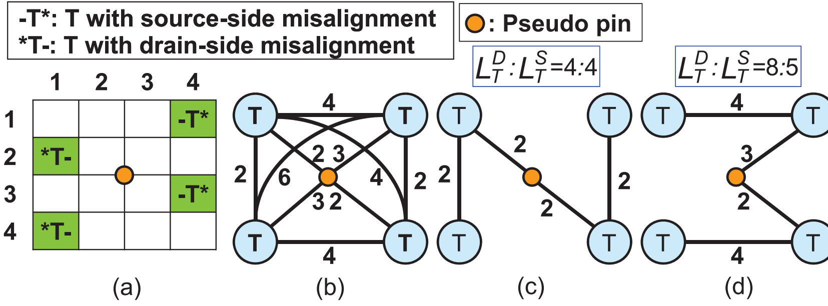

Fig. 11. An example of parasitic-aware routing for current-ratio matching. (a) A set of unit transistors with fixed orientation and positions. (b) The corresponding complete graph of (a). (c) The minimum spanning tree of (b). (d) The routing topology resulting in minimum current mismatch.

Table III. The Benchmark Circuits

Circuits	# of unit transistors
CM1	1, 1
CM2	1, 1, 2
CM3	1, 1, 2, 4
CM4	1, 1, 2, 4, 8
CM5	1, 1, 2, 4, 8, 16
CM6	1, 1, 2, 4, 8, 16, 32
CM7	1, 1, 2, 4, 8, 16, 32, 64
CM8	1, 1 ,2, 4, 8, 16, 32, 64, 128

maximize the matching of parasitic resistance. The best wirelength of t_i with the minimum $\epsilon_{(Ref)-(i)}$ in Equation (11) between t_{Ref} and t_i is chosen. By applying this topology refinement procedure for each scaled transistor, a common-centroid FinFET placement and routing with optimized matching of parasitic resistance can be generated.

Figure 11 demonstrates an example of the proposed parasitic-aware routing procedure for current-ratio matching. Given a set of unit transistors, T, with fixed orientations and positions, as seen in Figure 11(a), the corresponding complete graph can be constructed, as shown in Figure 11(b). Figure 11(c) shows the resulting MST, for which the wirelength ratio is {4:4}. After performing the wirelength refinement procedure for minimum current mismatch, a new routing topology with the best wirelength ratio, {8:5}, can be derived, as shown in Figure 11(d).

After performing the parasitic-aware routing, the global routing path of each net can be obtained. We then estimate the horizontal/vertical spacing between unit transistors according to the design rules and the number of required routing tracks in a horizontal/vertical channel. We keep the spacing as small as possible for better dispersion degree while satisfying common-centroid constraints.

5. EXPERIMENTAL RESULTS

We implemented the proposed common-centroid FinFET placement methodology in the MATLAB programming language on a personal computer with an Intel Core i7-2600 3.4GHz CPU and 16GB memory. We created a set of test cases of current mirrors, CM1, CM2, ..., CM8, with different width ratios of the transistors, as shown in the second column of Table III. To demonstrate the effectiveness of our approach, we conducted two sets of experiments: (1) applying different placement approaches with our

parasitic-aware routing approach, and (2) applying our parasitic-aware placement with parasitic-unaware and parasitic-aware routing approaches.

5.1. Applying Different Placement Approaches With Our Parasitic-Aware Routing Approach

For the first set of the experiment, we applied different placement approaches with the proposed parasitic-aware routing method. We compared our placement approach with that of Lin et al. [2011], which is known to be the most recent work in the literature handling common-centroid transistor placement with the considerations of diffusion sharing and dispersion and without the considerations of gate misalignment and parasitic resistance. Since the approach of Lin et al. [2011] does not include a router, we also performed our proposed parasitic-aware routing algorithm for their derived placements. To show the importance with and without considering parasitic resistance, we also compare our parasitic-aware placement approach with our ISPD work ("parasitic-unaware placement approach") [Wu et al. 2015]. For each current mirror, the expected current ratio must be equal to the unit transistor ratio. For each common-centroid FinFET layout generated by different approaches, we simulated the drain current of each transistor in the current mirror with the impact of gate misalignment and parasitic resistance according to Equation (4). We also evaluated the dispersion degree based on Equation (1) and the current mismatch based on Equation (10).

Table IV compares the simulated current ratio, current mismatch resulting from the impact of gate misalignment ("ϵ^G"), current mismatch resulting from the impact of parasitic resistance ("ϵ^P"), total current mismatch ("$\epsilon = \epsilon^G + \epsilon^P$"), dispersion degree ("$\rho$"), and runtime ("$T$") for different approaches. According to Table IV, with the consideration of gate misalignment, the parasitic-unaware placement approach can obtain a more accurate simulated current ratio than the approach of Lin et al. [2011] compared with the expected current ratio for all circuits. When comparing the evaluation metric of current mismatch with the approach of Lin et al. [2011], the parasitic-unaware placement approach can achieve up to 78% improvement, which is calculated by $\frac{\epsilon_2-\epsilon_1}{\epsilon_1}$. When considering both gate misalignment and parasitic resistance during common-centroid FinFET placement and routing, our parasitic-aware approach can derive the most accurate simulated current ratio compared with the expected current ratio for all circuits among these approaches. Moreover, our parasitic-aware approach can reduce up to 86% and 67% current mismatch compared with the approach of Lin et al. [2011] and the parasitic-unaware placement approach, which are calculated by $\frac{\epsilon_3-\epsilon_1}{\epsilon_1}$ and $\frac{\epsilon_3-\epsilon_2}{\epsilon_2}$, respectively. It should be noted that all ϵ^G values resulting from different approaches are the same, while the ϵ^P values resulting from different approaches are quite different because the current mismatch due to gate misalignment was considered in all placement approaches. Most of the ϵ^P values are negative because our proposed parasitic-aware routing approach can effectively adjust the routing wirelength to further reduce the current mismatch resulting from parasitic resistance. Consequently, it is necessary to apply both parasitic-aware placement and routing for better current matching, and our parasitic-aware placement is even better than the other two placement approaches.

In addition to much better current ratio matching resulting from our parasitic-aware placement and routing approach, both the parasitic-unaware placement approach and our parasitic-aware approach can obtain higher dispersion degree than the approach of Lin et al. [2011] in all circuits. We did not compare the layout area because the layout area resulting from different approaches for each circuit is the same. The runtimes based on three different approaches are similar. Figures 12(a)–(c) show the resulting common-centroid FinFET arrays of CM5 generated by different approaches, respectively.

Table IV. Comparisons of Simulated Current Ratio, Current Mismatch Resulting from the Impact of Gate Misalignment ("ϵ^G"), Current Mismatch Resulting from the Impact of Parasitic Resistance ("ϵ^P"), Total Current Mismatch ("$\epsilon = \epsilon^G + \epsilon^P$"), Dispersion Degree ("$\rho$"), and Runtime ("T") for Lin et al.'s and Our Approaches

Lin et al. [2011] + our parasitic-aware routing									
Circuits	Simulated current ratio	ϵ_1^G	ϵ_1^P	ϵ_1	ρ_1	T_1 (s)	Comparison (%) ϵ_1	ρ_1	T_1
CM1	1 : 1	0.00	0.00	0.00	0.90	0.00	-	-	-
CM2	1 : 1 : 2.19	0.21	−0.01	0.20	2.60	0.01	-	-	-
CM3	1 : 1 : 2.17 : 4.37	0.41	−0.04	0.37	5.26	0.01	-	-	-
CM4	1 : 1 : 2.17 : 4.39 : 8.06	0.62	−0.05	0.57	8.96	0.02	-	-	-
CM5	1 : 1 : 2.14 : 4.36 : 8.10 : 17.14	0.88	−0.14	0.73	12.85	0.05	-	-	-
CM6	1 : 1 : 2.14 : 4.39 : 8.12 : 17.25 : 33.20	1.14	−0.13	1.01	18.10	0.26	-	-	-
CM7	1 : 1 : 2.23 : 4.44 : 8.29 : 17.54 : 34.40 : 69.83	1.42	0.13	1.55	24.14	0.28	-	-	-
CM8	1 : 1.11 : 2.17 : 4.13 : 8.45 : 18.21 : 36.06 : 71.00 : 143.29	1.69	0.26	1.96	28.10	1.04	-	-	-

The parasitic-unaware placement approach [Wu et al. 2015] + our parasitic-aware routing									
Circuits	Simulated current ratio	ϵ_2^G	ϵ_2^P	ϵ_2	ρ_2	T_2 (s)	Comparison (%) $\frac{\epsilon_2-\epsilon_1}{\epsilon_1}$	$\frac{\rho_2-\rho_1}{\rho_1}$	$\frac{T_2-T_1}{T_1}$
CM1	1 : 1	0.00	0.00	0.00	0.90	0.00	0.00	0.00	0.00
CM2	1 : 1 : 2	0.21	−0.21	0.00	2.60	0.01	0.00	0.00	0.00
CM3	1 : 1 : 2.01 : 4.10	0.41	−0.33	0.08	5.26	0.02	−78.26	0.00	33.33
CM4	1 : 1 : 1.9883 : 4.06 : 8.23	0.62	−0.44	0.17	9.11	0.04	−69.79	1.70	100.00
CM5	1: 1 : 1.99 : 4.06 : 8.25 : 16.76	0.88	−0.52	0.36	13.04	0.08	−50.63	1.43	57.14
CM6	1 : 1 : 2.10 : 4.18 : 8.21 : 16.79 : 33.78	1.14	−0.56	0.58	19.18	0.28	−42.59	5.95	6.97
CM7	1 : 1 : 2.08 : 4.23 : 8.27 : 17.15 : 34.44 : 68.96	1.42	−0.36	1.06	24.60	0.32	−31.95	1.87	13.64
CM8	1 :1 : 2.02 : 4.09 : 8.29 : 16.93 : 34.08 : 68.32 : 137.15	1.69	−0.42	1.27	30.51	1.39	−34.90	8.57	33.20

Our parasitic-aware placement and routing approach									
Circuits	Simulated current ratio	ϵ_3^G	ϵ_3^P	ϵ_3	ρ_3	T_3 (s)	Comparison (%) $\frac{\epsilon_3-\epsilon_1}{\epsilon_1}$ $(\frac{\epsilon_3-\epsilon_2}{\epsilon_2})$	$\frac{\rho_3-\rho_1}{\rho_1}$ $(\frac{\rho_3-\rho_2}{\rho_2})$	$\frac{T_3-T_1}{T_1}$ $(\frac{T_3-T_2}{T_2})$
CM1	1 : 1	0.00	0.00	0.00	0.90	0.00	0.00 (0.00)	0.00 (0.00)	0.00 (0.00)
CM2	1 : 1 : 2	0.21	−0.21	0.00	2.60	0.01	0.00 (0.00)	0.00 (0.00)	0.00 (0.00)
CM3	1 : 1 : 2 : 4.06	0.41	−0.36	0.05	5.27	0.02	−85.84 (−34.84)	0.33 (0.33)	33.33 (0.00)
CM4	1 : 1 : 1.99 : 4.03 : 8.21	0.62	−0.48	0.14	8.96	0.04	−75.73 (−19.67)	0.03 (−1.64)	100.00 (0.00)
CM5	1 : 1 : 1.99 : 4.03 : 8.07 : 16.44	0.88	−0.69	0.19	13.17	0.08	−73.83 (−46.98)	2.45 (1.00)	57.14 (0.00)
CM6	1 : 1 :2.06 : 4.13 : 8.30 : 16.68 : 33.12	1.14	−0.73	0.41	19.18	0.29	−59.06 (−28.70)	5.94 (0.00)	10.55 (3.35)
CM7	1 : 1 : 2.08 : 4.13 : 8.22 : 16.36 : 33.14 : 65.95	1.42	−0.90	0.52	24.37	0.33	−66.38 (−50.59)	0.92 (−0.94)	17.00 (2.95)
CM8	1 : 1 : 2.01 : 4.03 : 8.02 : 16.05 : 32.91 : 64.92 : 130.80	1.69	−1.28	0.42	30.32	1.40	−78.74 (−67.34)	7.90 (−0.62)	35.00 (1.35)

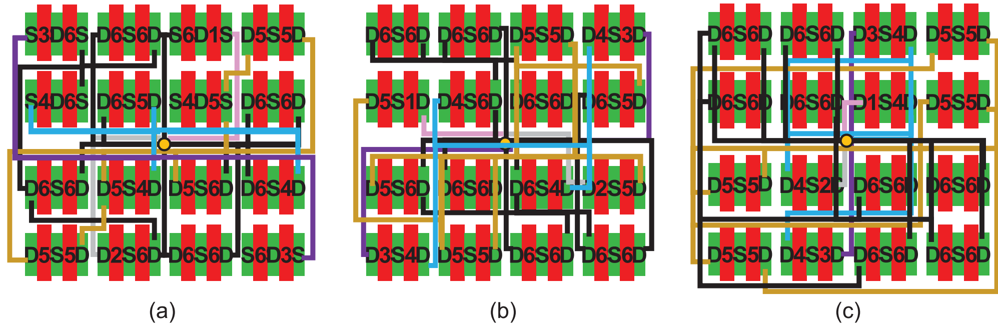

Fig. 12. The common-centroid FinFET layouts of CM5, which result from (a) the approach of Lin et al. [2011], (b) the parasitic-unaware placement approach, and (c) our parasitic-aware placement approach, respectively.

Table V. Comparisons of Simulated Current Ratio, Current Mismatch ("ϵ") and Runtime ("T") based on the Parasitic-Unaware Routing and Our Parasitic-Aware Routing

Our parasitic-aware placement approach + parasitic-unaware routing							
Circuits	Simulated current ratio	ϵ_4^G	ϵ_4^P	$\epsilon_4 = \epsilon_4^P + \epsilon_4^G$	T_4 (s)	Comparison (%) ϵ_4	Comparison (%) T_4
CM1	1 : 1	0.00	0.00	0.00	0.00	-	-
CM2	1 : 1 : 2	0.21	−0.21	0.00	0.00	-	-
CM3	1 : 1 : 2.00 : 4.09	0.41	−0.35	0.06	0.01	-	-
CM4	1: 1 : 1.99 : 4.08 : 8.31	0.62	−0.41	0.21	0.03	-	-
CM5	1 : 1 : 1.99 : 4.08 : 8.28 : 16.72	0.88	−0.51	0.36	0.05	-	-
CM6	1 : 1 : 2.07 : 4.15 : 8.37 : 16.78 : 33.61	1.14	−0.62	0.52	0.24	-	-
CM7	1 : 1 : 2.09 : 4.18 : 8.37 : 16.76 : 33.66 : 67.35	1.42	−0.78	0.64	0.28	-	-
CM8	1 : 1 : 2.01 : 4.11 : 8.29 : 16.75 : 33.60 : 67.29 : 134.65	1.69	−0.75	0.94	1.34	-	-

Our parasitic-aware placement and routing approach							
Circuits	Simulated current ratio	ϵ_3^G	ϵ_3^P	$\epsilon_3 = \epsilon_3^P + \epsilon_3^G$	T_3 (s)	Comparison (%) $\frac{\epsilon_3-\epsilon_4}{\epsilon_4}$	Comparison (%) $\frac{T_3-T_4}{T_4}$
CM1	1 : 1	0.00	0.00	0.00	0.00	0.00	0.00
CM2	1 : 1 : 2	0.21	−0.21	0.00	0.01	0.00	0.00
CM3	1 : 1 : 2 : 4.06	0.41	−0.36	0.05	0.02	−18.42	100.00
CM4	1 : 1 : 1.99 : 4.03 : 8.21	0.62	−0.48	0.14	0.04	−33.17	44.54
CM5	1:1:1.99:4.03:8.07:16.44	0.88	−0.69	0.19	0.08	−47.17	60.85
CM6	1 : 1 :2.06 : 4.13 : 8.30 : 16.68 : 33.12	1.14	−0.73	0.41	0.29	−20.65	18.99
CM7	1 : 1 : 2.08 : 4.13 : 8.22 : 16.36 : 33.14 : 65.95	1.42	−0.90	0.52	0.33	−18.02	15.74
CM8	1 : 1 : 2.01 : 4.03 : 8.02 : 16.05 : 32.91 : 64.92 : 130.80	1.69	−1.28	0.42	1.40	−55.90	4.98

5.2. Applying Our Parasitic-Aware Placement With Parasitic-Unaware and Parasitic-Aware Routing Approaches

For the second set of the experiment, we applied the proposed parasitic-aware placement method with both parasitic-unaware and parasitic-aware routing approaches. As mentioned in Section 4.4, our parasitic-aware routing approach starts with the MST algorithm, then iteratively exchanges different edges based on the nondecreasing order of the routing wirelength to further adjust the routing topology while maximizing the matching of parasitic resistance. To show the effectiveness of the proposed approach, in this experiment, the parasitic-unaware routing approach was simply implemented based on the MST algorithm such that we can observe the difference before and after the routing topology refinement for optimizing current ratio matching.

Table V compares the simulated current ratio, current mismatch ("ϵ") and runtime ("T") for the two approaches. According to Table V, with the consideration of parasitic

resistance during common-centroid routing, our parasitic-aware placement and routing approach can obtain more accurate simulated current ratio than our parasitic-aware placement approach + parasitic-unaware routing compared with the expected current ratio for all circuits. When comparing the evaluation metric of current mismatch, our parasitic-aware placement and routing approach can achieve up to 56% improvement, which is calculated by $\frac{\epsilon_3-\epsilon_4}{\epsilon_4}$. We did not compare the dispersion degree and layout area because both resulting from different approaches for each circuit are the same. The runtime based on both approaches are very similar, which indicates that the proposed routing topology refinement method is very efficient. Consequently, our parasitic-aware routing approach is very effective and efficient to maximize the matching of parasitic resistance for better current ratio matching.

6. CONCLUSIONS

In this article, we have introduced the importance of considering gate misalignment and parasitic resistance during common-centroid FinFET placements and routings. We have proposed a novel approach to generate common-centroid FinFET placement and routing with the consideration of gate misalignment and parasitic resistance, atogether with all the conventional common-centroid rules. Experimental results have shown that the proposed placement and routing approach can effectively minimize current mismatch resulting from gate misalignment and parasitic resistance, and simultaneously maximize the dispersion degree of a common-centroid FinFET array.

REFERENCES

L. Baldi, B. Franzini, D. Pandini, and R. Zafalon. 2001. Design solutions for the interconnection parasitic effects in deep sub-micron technologies. *Microelectronic Engineering* 55, 1–4, 11–18.

T. Chiarella, L. Witters, A. Mercha, C. Kerner, M. Rakowski, C. Ortolland, L.-A. Ragnarsson, B. Parvais, A. De Keersgieter, S. Kubicek, A. Redolfi, C. Vrancken, S. Brus, A. Lauwers, P. Absil, S. Biesemans, and T. Hoffmann. 2010. Benchmarking SOI and bulk FinFET alternatives for PLANAR CMOS scaling succession. *Solid-State Electronics* 54, 9, 855–860.

T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. 2001. *Introduction to Algorithms* (2nd ed.). MIT Press, Cambridge, MA, and McGraw-Hill Book Co., Burr Ridge, IL.

R. Dreslinski, M. Wiekowski, D. Blaauw, D. Sylvester, and T. Mudge. 2010. Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits. In *Proceedings of the IEEE*. 253–266.

M. Fulde, A. Mercha, C. Gustin, B. Parvais, V. Subramanian, K. von Arnim, F. Bauer, K. Schruefer, D. Schmitt-Landsiedel, and G. Knoblinger. 2007. Analog design challenges and trade-offs using emerging materials and devices. In *Proceedings of IEEE European Solid State Device Research Conference*. 123–126.

A. Hastings. 2006. *The Art of Analog Layout* (2nd ed.). Prentice Hall, Upper Saddle River, NJ.

K.-H. Ho, H.-C. Ou, Y.-W. Chang, and H.-F. Tsao. 2013. Coupling-aware length-ratio-matching routing for capacitor arrays in analog integrated circuits. In *Proceedings of ACM/IEEE Design Automation Conference*. 1–6.

C.-C. Huang, C.-L. Wey, J.-E. Chen, and P.-W. Luo. 2013. Optimal common-centroid-based unit capacitor placements for yield enhancement of switched-capacitor circuits. *ACM Transactions on Design Automation of Electronic Systems* 19, 1, (Dec. 2013), 7:1–7:13.

Intel. 2011. Intel's Revolutionary–22 nm Transistor Technology. Retrieved March 24, 2016 from http://www.intel.com.

ITRS. 2012. International Technology Roadmap for Semiconductors. Retrieved March 24, 2016 from http://www.itrs.net/home.html.

Y. Li, Z. Zhang, D. Chua, and Y. Lian. 2014. Placement for binary-weighted capacitive array in SAR ADC using multiple weighting methods. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 33, 9, 1277–1287.

C.-W. Lin, C.-L. Lee, J.-M. Lin, and S.-J. Chang. 2012a. Analytical-based approach for capacitor placement with gradient error compensation and device correlation enhancement in analog integrated circuits. In *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*. 635–642.

C.-W. Lin, J.-M. Lin, Y.-C. Chiu, C.-P. Huang, and S.-J. Chang. 2012b. Mismatch-aware common-centroid placement for arbitrary-ratio capacitor arrays considering dummy capacitors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 31, 12, 1789–1802.

M. P.-H. Lin, Y.-T. He, V. W.-H. Hsiao, R.-G. Chang, and S.-Y. Lee. 2013. Common-centroid capacitor layout generation considering device matching and parasitic minimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 32, 7, 991–1002.

M. P.-H. Lin, V. W.-H. Hsiao, and C.-Y. Lin. 2014. Parasitic-aware sizing and detailed routing for binary-weighted capacitors in charge-scaling DAC. In *Proceedings of ACM/IEEE Design Automation Conference*. 1–6.

M. P.-H. Lin, H. Zhang, M. D. F. Wong, and Y.-W. Chang. 2009. Thermal-driven analog placement considering device matching. In *Proceedings of ACM/IEEE Design Automation Conference*. 593–598.

M. P.-H. Lin, H. Zhang, M. D. F. Wong, and Y.-W. Chang. 2011. Thermal-driven analog placement considering device matching. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 30, 3, 325–336.

P.-H. Lin, H.-C. Yu, T.-H. Tsai, and S.-C. Lin. 2007. A matching-based placement and routing system for analog design. In *Proceedings of IEEE International Symposium on VLSI Design, Automation and Test*. 1–4.

W. Liu, X. Jin, J. Chen, M.-C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P. K. Ko, and Chenming Hu. 1998. *BSIM 3v3.2 MOSFET Model Users' Manual*. Technical Report UCB/ERL M98/51. EECS Department, University of California, Berkeley. Retrieved March 24, 2016 from http://www.eecs.berkeley.edu/Pubs/TechRpts/1998/3486.html.

D. Long, X. Hong, and S. Dong. 2005. Optimal two-dimension common centroid layout generation for MOS transistors unit-circuit. In *Proceedings of the IEEE International Symposium on Circuits and Systems*. 2999–3002.

P.-W. Luo, J.-E. Chen, C.-L. Wey, L.-C. Cheng, J.-J. Chen, and W.-C. Wu. 2008. Impact of capacitance correlation on yield enhancement of mixed-signal/analog integrated circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 27, 11, 2097–2101.

Q. Ma, L. Xiao, Y. C. Tam, and E. F. Y. Young. 2011. Simultaneous handling of symmetry, common centroid, and general placement constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 30, 1, 85–95.

Q. Ma, E. F. Y. Young, and K. P. Pun. 2007. Analog placement with common centroid constraints. In *Proceedings of ACM/IEEE International Conference on Computer-Aided Design*. 579–585.

R. Naiknaware and T. S. Fiez. 1999. Automated hierarchical CMOS analog circuit stack generation with intramodule connectivity and matching considerations. *IEEE Journal of Solid-State Circuits* 34, 3, 304–303.

P. R. J. Östergård. 2001. A new algorithm for the maximum-weight clique problem. *Nordic Journal of Computing* 8, 4, 424–436.

S. H. Rasouli, K. Endo, and K. Banerjee. 2009. Variability analysis of FinFET-based devices and circuits considering electrical confinement and width quantization. In *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*. 505–512.

B. Razavi. 2000. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Book Co., Burr Ridge, IL.

S. Sarangia, S. Bhushana, A. Santraa, S. Dubeyb, S. Jitb, and P. K. Tiwari. 2013. A rigorous simulation based study of gate misalignment effects in gate engineered double-gate (DG) MOSFETs. *Superlattices and Microstructures* 60, 0, 263–279.

V. Subramanian, B. Parvais, J. Borremans, A. Mercha, D. Linten, P. Wambacq, J. Loo, M. Dehan, C. Gustin, N. Collaert, S. Kubicek, R. Lander, J. Hooker, F. Cubaynes, S. Donnay, M. Jurczak, G. Groeseneken, Willy Sansen, and S. Decoutere. 2006. Planar bulk MOSFETs versus FinFETs: An analog/RF perspective. *IEEE Transactions on Electron Devices* 53, 12, 3071–3079.

R. Valin, C. Sampedro, M. Aldegunde, A. Garcia-Loureiro, N. Seoane, A. Godoy, and F. Gamiz. 2012. Two-dimensional Monte Carlo simulation of DGSOI MOSFET misalignment. *IEEE Transactions on Electron Devices* 59, 6, 1621–1628.

P. Wambacq, B. Verbruggen, K. Scheir, J. Borremans, M. Dehan, D. Linten, V. De Heyn, G. Van der Plas, A. Mercha, B. Parvais, C. Gustin, V. Subramanian, N. Collaert, M. Jurczak, and S. Decoutere. 2007. The potential of FinFETs for analog and RF circuit applications. *IEEE Transactions on Circuits and Systems: Regular Papers* 54, 11, 2541–2551.

P.-H. Wu, M. P.-H. Lin, X. Li, and T.-Y. Ho. 2015. Common-centroid FinFET placement considering the impact of gate misalignment. In *Proceedings of ACM International Symposium on Physical Design*. 25–31.

L. Xiao and E. F. Y. Young. 2009. Analog placement with common centroid and 1-D symmetry constraints. In *Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference*. 353–360.

T. Yan, S. Nakatake, and T. Nojima. 2006. Formulating the empirical strategies in module generation of analog MOS layout. In *Proceedings of the IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures*. 44–49.

L. Zhang, S. Dong, Y. Ma, and X. Hong. 2010. Multi-stage analog placement with various constraints. In *Proceedings of IEEE International Conference on Communications, Circuits and Systems*. 881–885.

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