Common-Centroid FinFET Placement Considering the Impact of Gate Misalignment*

Po-Hsun Wu[1], Mark Po-Hung Lin[2], X. Li[3], and Tsung-Yi Ho[4]
[1]Department of Computer Science and Information Engineering, National Cheng Kung University, Tainan, Taiwan
[2]Department of Electrical Engineering and AIM-HI, National Chung Cheng University, Chiayi, Taiwan
[3]Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA 15213, USA
[4]Department of Computer Science, National Chiao Tung University, Hsinchu, Taiwan
devilangel@eda.csie.ncku.edu.tw; marklin@ccu.edu.tw; xinli@cmu.edu; tyho@cs.nctu.edu.tw

ABSTRACT

The FinFET technology has been regarded as a better alternative among different device technologies at 22nm node and beyond due to more effective channel control and lower power consumption. However, the gate misalignment problem resulting from process variation based on the FinFET technology becomes even severer compared with the conventional planar CMOS technology. Such misalignment may increase the threshold voltage and decrease the drain current of a single transistor. When applying the FinFET technology to analog circuit design, the variation of drain currents will destroy the current matching among transistors and degrade the circuit performance. In this paper, we present the first FinFET placement technique for analog circuits considering the impact of gate misalignment together with systematic and random mismatch. Experimental results show that the proposed algorithms can obtain an optimized common-centroid FinFET placement with much better current matching.

Categories and Subject Descriptors
B.7.2 [Integrated Circuits]: Design Aids - Placement and Routing; Layout.

General Terms
Algorithms, Design.

Keywords
Analog placement; FinFET; gate misalignment; common centroid.

1. INTRODUCTION

In modern system-on-chip (SoC) design, the voltage of a transistor has been aggressively operated from the traditional super-threshold region to the sub/near-threshold region to effectively reduce power consumption of integrated circuits [4]. As the conventional planar CMOS technology scales down to the $22nm$ node and beyond, it becomes more and more challenging to effectively control short channel effects (SCEs) [1]. As a result, high leakage current and threshold voltage variation will significantly affect the circuit performance, power dissipation, and reliability of circuits.

To overcome the difficulty of planar CMOS scaling, several new device technologies have been developed as alternatives of the bulk-silicon MOSFET structure for improved reliability. Among those device technologies, the Fin Field Effect Transistor (FinFET) has been regarded as one of the most promising technologies to substitute the bulk-silicon MOSFET for ultimate scaling [2]. As the three-dimensional (3-D) structure of FinFETs can better control the drain-source channel, the leakage current can be significantly reduced due to the alleviation of SCEs. In addition, the threshold voltage variation can also be reduced by near-intrinsic channel doping due to random dopant fluctuations [21]. Owing to the reduction of both leakage current and threshold voltage based on the FinFET technology, it had been suggested to design analog integrated circuits with FinFETs for greater improvement of power, performance, and chip area [25].

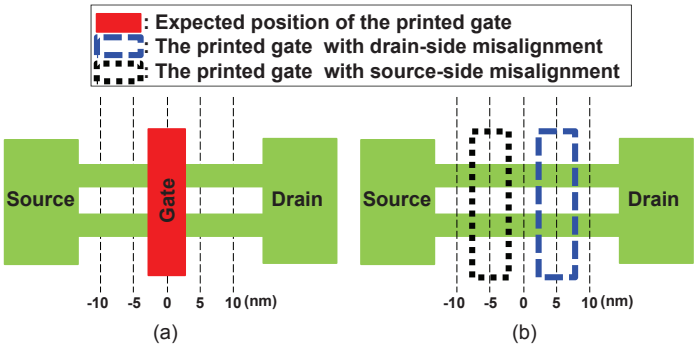

Figure 1: An example of gate misalignment of a FinFET [24]. (a) An ideal FinFET without gate misalignment. (b) A real FinFET with either drain-side or source-side gate misalignment.

Although the FinFET technology can effectively minimize the impact from SCEs and benefit power, performance, and chip area of integrated circuits, some lithography-induced process variation, such as gate misalignment, becomes even more severe. Due to the gate misalignment, the position of the printed gate of a FinFET may be deviated from the expected position after a set of lithography processes, which will increase the threshold voltage and decrease the drain current of the FinFET [5, 23, 24]. Figure 1 illustrates an example of gate misalignment. Ideally, the gate of a FinFET is expected to be located at the center between source and drain, as shown in Figure 1(a). However, the printed gate is usually misaligned due to process variation, as shown in Figure 1(b). Accord-

*This work was partially supported by the Ministry of Science and Technology of Taiwan, under Grant No's. NSC 102-2220-E-194-006, NSC 102-2221-E-194-065-MY2, and NSC 103-2917-I-006-086.

ISPD'15, March 29–April 1, 2015, Monterey, CA, USA.

http://dx.doi.org/10.1145/2717764.2717769.

ing to [24], the misaligned distance can be as large as $5nm$ either to the source side or the drain side for a $10nm$ process technology.

Sarangia *et al.* [23] reported that the threshold voltage of a FinFET, V_{th}, is more sensitive with source-side misalignment than with drain-side misalignment. When the gate is misaligned to the drain side of a FinFET by $5nm$ in the worst case, V_{th} will be increased by 0.01V. On the other hand, when the gate is misaligned to the source side a FinFET by $5nm$, V_{th} will be increased by 0.05V. Such increment will significantly degrade the drain current of the FinFET by 40% with a supply voltage of 1V. As most of the analog building blocks, such as current mirrors and differential pairs, are very sensitive to the current variation or current mismatch, it is essential to consider the impact of gate misalignment during the layout design of those building blocks. It should be noted that during IC fabrication, the direction and distance of gate misalignment of different FinFETs on the same chip are usually the same. What designers need to do is to carefully arrange the orientations of all FinFETs within a current mirror or a differential pair such that the ratio of the drain current among different transistors in a current mirror or a differential pair can be perfectly matched [5].

To generate a matched layout of the transistors in a current mirror or a differential pair, all the previous works [13, 14, 16, 18, 19, 26, 27, 28] simply followed the general common-centroid rules, including coincidence, symmetry, dispersion, and compactness [6]. None of them considered the impact of gate misalignment arising from the FinFET technology. Although Long *et. al.* [16] mentioned the chirality condition of transistors within a common-centroid structure, such chirality condition cannot achieve the best current matching with the impact of gate misalignment. Other recent works [7, 8, 9, 10, 11, 12] focus on the optimization of common-centroid capacitor placement, but the capacitors in these works are still not associated with the FinFET technology.

Different from all the previous works, we present the *first* problem formulation in the literature for common-centroid FinFET placement with the consideration of the impact of gate misalignment. Our contributions are summarized as follows:

- We propose a novel common-centroid FinFET placement formulation which simultaneously considers all the conventional common-centroid rules, including coincidence, symmetry, dispersion, and compactness, and the impact of gate misalignment for next generation analog layout design.
- We derive a new quality metric for evaluating the matching quality of drain currents of different transistors in a current mirror on the existence of gate misalignment within a common-centroid FinFET array.
- Based on the quality metric and the spatial correlation model, we present the common-centroid FinFET placement flow and algorithms to optimize the orientations of all sub-transistors and maximize the dispersion degree of a common-centroid FinFET array.
- Our experimental results show that the proposed common-centroid FinFET placement approach can achieve much better current matching among transistors in a current mirror on the existence of gate misalignment while maintaining high dispersion degree.

The rest of this paper is organized as follows: Section 2 introduces the common-centroid FinFET placement of a current mirror, and reviews the spatial correlation model for evaluating the dispersion degree of a common-centroid FinFET placement. Section 3 demonstrates the current mismatch resulting from the impact of gate misalignment. Section 4 details the proposed common-centroid FinFET placement algorithms. Section 5 shows the experimental results, and Section 6 concludes this paper.

2. PRELIMINARIES

A current mirror, as shown in Figure 2(a), is one of the most important basic building blocks in many analog circuit components. It produces a constant replicated current, I_{Copy}, flowing through a scaled transistor regardless of its loading by copying the reference current, I_{Ref}, flowing through another reference transistor. If the size, or the channel width, of the scaled transistor is n times larger than that of the reference transistor, I_{Copy} will be also scaled by a factor of n with respect to I_{Ref}. A current mirror may have several replicated currents with different scaling factors.

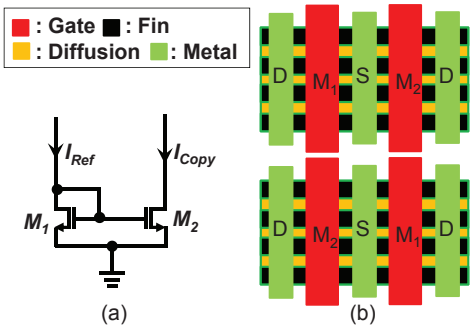

Figure 2: (a) A current mirror, where the size of the transistors, M_1 and M_2, are the same. (b) An example common-centroid FinFET placement of the current mirror in (a), where M_1 and M_2 are split into two sub-transistors with the same number of fins, respectively.

When generating a common-centroid placement of a current mirror, it is required to optimize the matching quality among the reference transistor and all the other scaled transistors for accurate scaling factors. According to [10], the mismatch occurs due to process variation can be divided into two categories: systematic mismatch and random mismatch. To reduce systematic mismatch, each transistor is split into several smaller sub-transistors of the same size, and each sub-transistor should be placed symmetrically with respect to a common center point, as shown in Figure 2(b), where each transistor in Figure 2(a) is divided into two sub-transistors.

On the other hand, random mismatch is mainly related with statistical fluctuations in processing conditions or material properties. Because these fluctuations are in random mechanisms, all sub-transistors of each transistor should be distributed throughout a layout to reduce random mismatch. In other words, all sub-transistors should exhibit the highest degree of dispersion in a common-centroid sub-transistor array [22]. A spatial correlation model [10, 17] had been proposed in the literature to measure the dispersion degree of a common-centroid placement.

Assume that a set of sub-transistors of all transistors are arranged in an $r \times c$ matrix. For any two sub-transistors, st_i and st_j, which are located at the entries in the r_i^{th} row and c_i^{th} column and the r_j^{th} row and c_j^{th} column, their correlation coefficient ρ_{ij} is defined in Equation (1).

$$\rho_{ij} = \rho_u^{D(i,j)}, \tag{1}$$

where $0 < \rho_u < 1$, and $D(i,j) = \sqrt{(r_i - r_j)^2 + (c_i - c_j)^2} \times l$. l depends on process and size of transistors. According to [17],

they assume that ρ_u = 0.9 and l = 1 to observe the relation between correlation and mismatch.

Let L denotes the overall correlation coefficient, or the dispersion degree, of a common-centroid placement. For n transistors, L is the summation of all correlation coefficients of a pair of transistors and is defined as Equation (2).

$$L = \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} R_{ij}, \tag{2}$$

where R_{ij} is the correlation coefficient of two transistors, t_i and t_j. Assume that t_i consists of n_i sub-transistors and t_j consists of n_j sub-transistors. R_{ij} can be calculated by Equation (3).

$$R_{ij} = \frac{\sum_{a=1}^{n_i} \sum_{b=1}^{n_j} \rho_{ab}}{\sqrt{X \times Y}}, \tag{3}$$

where $X = n_i + 2\sum_{a=1}^{n_i-1} \sum_{b=a+1}^{n_i} \rho_{ab}$,
and $Y = n_j + 2\sum_{a=1}^{n_j-1} \sum_{b=a+1}^{n_j} \rho_{ab}$.

Based on the above mathematical model, we want to generate common-centroid placement with larger L for higher dispersion degree.

3. CURRENT MISMATCH DUE TO GATE MISALIGNMENT

As mentioned in Section 1, the gate misalignment problem based on the FinFET technology may have great impact on drain currents among different transistors in a current mirror. In addition to maximizing the dispersion degree of a common-centroid placement for minimizing random mismatch, it is required to study how to evaluate the matching quality of current ratios resulting from a common-centroid placement with known orientations of all sub-transistors within a common-centroid FinFET array on the existence of gate misalignment.

In this section, we will first derive the quality metric for evaluating the current mismatch of a current mirror on the existence of gate misalignment within a common-centroid FinFET array, and then give a case study to show the importance of determining the orientation of each transistor during common-centroid placement for minimizing the impact of gate misalignment.

3.1 Evaluation of Current Mismatch

We are given a set of k transistors and each transistor, t_i, contains n_i sub-transistors with determined orientations. Due to the impact of gate misalignment, the threshold voltage of the sub-transistors with drain-side misalignment is V_{th}^d and the threshold voltage of the sub-transistors with source-side misalignment is V_{th}^s. The resulting current ratio, $I_{n_1} : I_{n_2} : \ldots : I_{n_k}$, of these transistors with the impact of gate misalignment can be expressed, as given in Equation (4):

$$\begin{aligned} I_{n_1} : I_{n_2} : ... : I_{n_k} = n_1 : n_2 : ... : n_k = \\ (n_1^d \times f(V_{th}^d) + n_1^s \times f(V_{th}^s)) : \\ (n_2^d \times f(V_{th}^d) + n_2^s \times f(V_{th}^s)) : ... : \\ (n_k^d \times f(V_{th}^d) + n_k^s \times f(V_{th}^s)), \end{aligned} \tag{4}$$

where n_i^d denotes the number of sub-transistors of t_i with drain-side misalignment, and n_i^s denotes the number of sub-transistors of t_i with source-side misalignment (i.e., $n_i = n_i^d + n_i^s$), and $f(x)$ is a function of drain current based on given voltage x.

Based on the multiplication property of equality, we can derive the expression in Equation (5):

$$\begin{aligned} \frac{1}{n_1} \times (n_1^d \times f(V_{th}^d) + n_1^s \times f(V_{th}^s)) = \\ \frac{1}{n_2} \times (n_2^d \times f(V_{th}^d) + n_2^s \times f(V_{th}^s)) = ... = \\ \frac{1}{n_k} \times (n_k^d \times f(V_{th}^d) + n_k^s \times f(V_{th}^s)). \end{aligned} \tag{5}$$

After splitting the Equation (5), we can obtain a set of $k \times (k-1)$ equalities, as shown in Equation (6):

$$\begin{aligned} \frac{1}{n_1} \times (n_1^d \times f(V_{th}^d) + n_1^s \times f(V_{th}^s)) = \\ \frac{1}{n_2} \times (n_2^d \times f(V_{th}^d) + n_2^s \times f(V_{th}^s)), \\ \frac{1}{n_1} \times (n_1^d \times f(V_{th}^d) + n_1^s \times f(V_{th}^s)) = \\ \frac{1}{n_3} \times (n_3^d \times f(V_{th}^d) + n_3^s \times f(V_{th}^s)), ..., \\ \frac{1}{n_{k-2}} \times (n_{k-2}^d \times f(V_{th}^d) + n_{k-2}^s \times f(V_{th}^s)) = \\ \frac{1}{n_k} \times (n_k^d \times f(V_{th}^d) + n_k^s \times f(V_{th}^s)), \\ \frac{1}{n_{k-1}} \times (n_{k-1}^d \times f(V_{th}^d) + n_{k-1}^s \times f(V_{th}^s)) = \\ \frac{1}{n_k} \times (n_k^d \times f(V_{th}^d) + n_k^s \times f(V_{th}^s)). \end{aligned} \tag{6}$$

By substituting $n_i = n_i^d + n_i^s$ into the above equalities and simplifying the equalities, a set of equations can be derived, as shown in Equation (7):

$$\begin{aligned} \frac{|f(V_{th}^s) - f(V_{th}^d)| \times |n_1^d \times n_2^s - n_2^d \times n_1^s|}{n_1 \times n_2} = \epsilon_{1-2}, \\ \frac{|f(V_{th}^s) - f(V_{th}^d)| \times |n_1^d \times n_3^s - n_3^d \times n_1^s|}{n_1 \times n_3} = \epsilon_{1-3}, ..., \\ \frac{|f(V_{th}^s) - f(V_{th}^d)| \times |n_{k-1}^d \times n_k^s - n_k^d \times n_{k-1}^s|}{n_k \times n_{k-1}} = \epsilon_{(k-1)-(k)}, \end{aligned} \tag{7}$$

where ϵ_{i-j} denotes the current mismatch between two transistors, t_i and t_j, and $0 \leq \epsilon_{i-j} \leq 1$. If the resulting current ratio equals to the expected current ratio (i.e., no current mismatch), ϵ_{i-j} will be equal to 0.

Consequently, the overall current mismatch among different transistors in a current mirror, ϵ, can be obtained by summing up all ϵ_{i-j}, as seen in Equation (8):

$$\begin{aligned} \epsilon &= \epsilon_{1-2} + \epsilon_{1-3} + ... + \epsilon_{(k-1)-(k)} \\ &= \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \epsilon_{i-j} \\ &= \sum_{i=1}^{k-1} \sum_{j=i+1}^{k} \left(\frac{|f(V_{th}^d) - f(V_{th}^s)| \times |n_i^d \times n_j^s - n_j^d \times n_i^s|}{n_i \times n_j}\right). \end{aligned} \tag{8}$$

3.2 A Case Study

We conduct a case study, as demonstrated in Figure 3, for the following purposes: (1) comparing different common-centroid placements with and without considering the impact of gate misalign-

Table 1: Comparisons of the simulated current ratios, current mismatch (ϵ) and dispersion degree (L) for different common-centroid placements in Figures 3(b)–(d).

Test Case	# of Sub-transistors	Simulated Current Ratio	ϵ	L
Figure 3(b)	2, 2, 4, 8	1.00 : 0.93 : 2.07 : 4.00	0.16	5.6827
Figure 3(c)		1.00 : 0.93 : 1.93 : 4.14	0.17	5.7338
Figure 3(d)		1.00 : 1.00 : 2.00 : 4.00	0.00	5.7459

ment and dispersion, (2) evaluating the resulting current mismatch and dispersion degree of each common-centroid placement, and (3) justifying the correctness of Equation (8) based on circuit simulation.

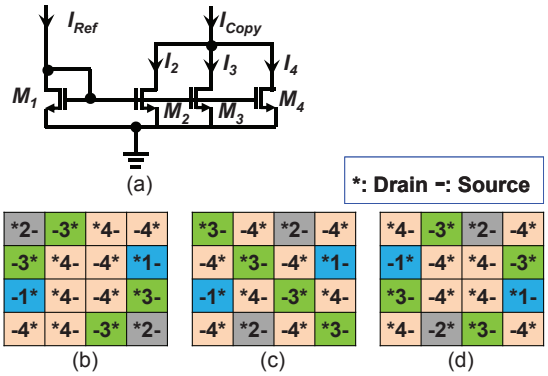

Figure 3: Comparisons of different common-centroid FinFET placements. (a) A current mirror with the idea current ratio, I_{Ref} : I_2 : I_3 : I_4 is 1 : 1 : 2 : 4. (b) A common-centroid FinFET placement for the current mirror in (a) without considering both gate misalignment and dispersion. (c) A common-centroid FinFET placement for the current mirror in (a) with the consideration of dispersion. (d) A common-centroid FinFET placement for the current mirror in (a) with the considerations of both gate misalignment and dispersion.

The current mirror in Figure 3(a) consists of four transistors. The reference current, I_{Ref}, flows through the reference transistor, M_1, and the replicated currents, I_2, I_3, and I_4, are copied from I_{Ref} to other three transistors, M_2, M_3, and M_4 with different scaling factors. The scaling factors, or the number of sub-transistors of M_1, M_2, M_3, and M_4 are 2, 2, 4, and 8, respectively, so the ideal current ratio, I_{Ref} : I_2 : I_3 : I_4, is 1 : 1 : 2 : 4. Figures 3(b)–(d) give three different common-centroid FinFET placements for the current mirror in Figure 3(a) with and without considering gate misalignment and dispersion.

For each common-centroid placement in Figure 3, we evaluate the dispersion degree and current mismatch based on Equations (2) and (8), and observe the resulting drain current of each transistor by performing SPICE simulation based on the BSIM-CMG model [15]. Without loss of generality, we assume that the printed gates of all sub-transistors in each common-centroid placement are misaligned to the right side, so the printed gate of a sub-transistor will have either drain-side or source-side misalignment according to its orientation. As mentioned in Section 1, in the worst case, V_{th} is increased by 0.01V with drain-side misalignment and increased by 0.05V with source-side misalignment based on a $10nm$ FinFET technology with 1V supply voltage, and hence the function, $|f(V_{th}^d - f(V_{th}^s)|$, in Equation (8) is equal to 0.069 (A). We also adopt these settings to adjust the threshold voltage of each sub-transistor for SPICE simulation.

Table 1 reports the resulting simulated current ratio, current mismatch (ϵ), and dispersion degree (L) for each common centroid placement in Figures 3(b)–(d). According to the Table 1, the common-centroid FinFET placement in Figure 3(b) without considering both gate misalignment and dispersion results in worse dispersion degree and current ratio matching. The common-centroid FinFET placement in Figure 3(c), with the only consideration of dispersion and without considering the impact of gate misalignment, results in better dispersion degree, but the worst current ratio matching. The common-centroid FinFET placement in Figure 3(d) with the considerations of both gate misalignment and dispersion results in the best dispersion degree and current ratio matching. Consequently, it is very important to consider both gate misalignment and dispersion to effectively reduce the current mismatch and to maximize the dispersion degree. The current mismatch due to gate misalignment can be eliminated if the orientation of each sub-transistor is carefully arranged.

4. COMMON-CENTROID FINFET PLACEMENT ALGORITHMS

Based on the evaluation metrics of dispersion degree and current mismatch in Equations (2) and (8), in this section, we propose our algorithms to generate an optimized common-centroid FinFET placement with the considerations of the impact of gate misalignment and dispersion. Our approach starts with the determination of sub-transistor orientations, which is detailed in Section 4.1. Based on the determined orientations, an initial common-centroid FinFET placement is then generated by maximizing diffusion sharing and dispersion degree in each row, which is illustrated in Section 4.2. A final placement refinement is done by a shortest path formulation for maximizing the dispersion degree among sub-transistors in different rows, which is described in Section 4.3.

4.1 Determination of Sub-transistor Orientations

As explained in the previous section, to reduce the current mismatch, the orientation of the sub-transistors must be properly determined. We formulate the problem as finding the minimum-weight clique [3] in an undirected graph to simultaneously determine the orientation of all sub-transistors. Each vertex in the graph represents one configuration of the sub-transistor orientations of a transistor, t_i, which has n_i^s sub-transistors with source-side misalignment and n_i^d sub-transistors with drain-side misalignment, respectively. There exists an edge between two vertices if the vertices correspond to two different transistors, t_i and t_j. The edge weight, ϵ_{i-j}, which can be calculated by Equation (7), denotes the current mismatch between t_i and t_j based on the configurations of sub-transistor orientations represented by the vertices. We enumerate all possible configurations (i.e., a k-finger FinFET have k+1 configurations whose orientations are the combination of source-side misalignment and drain-side misalignment) of sub-transistor orientations for each transistor in the graph. Figure 4 shows an minimum-weight-clique formulation for a current mirror with three

transistors, A, B, and C, where each transistor has 2, 2, and 3 possible configurations of sub-transistor orientations, respectively. By finding the minimum-weight clique in the undirected graph, the best configuration of sub-transistor orientations for each transistor can be determined such that the minimum current mismatch can be achieved.

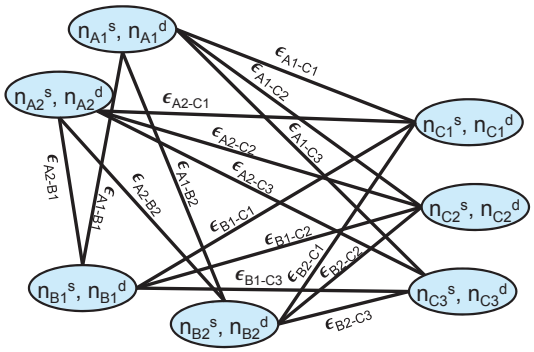

Figure 4: An example minimum-weight-clique formulation for a current mirror with three transistors, A, B, and C, where each transistor has 2, 2, and 3 possible configurations of sub-transistor orientations, respectively.

4.2 Common-Centroid FinFET Placement Considering Dispersion and Diffusion Sharing

After determining the sub-transistor orientations, we want to generate a common-centroid FinFET placement while maintaining the sub-transistor orientations and maximizing the dispersion degree. When generating an m-row common-centroid FinFET placement, we first evenly distribute all sub-transistors of each transistor to the m rows such that the dispersion degree of a common-centroid FinFET placement can be effectively maximized in the subsequent steps. Given a set of n_i sub-transistors of a transistor, t_i, we assign $\frac{n_i}{m}$ sub-transistors into each row. If n_i is less than m, we randomly assign the sub-transistors into different rows while keeping the numbers of sub-transistors in different rows the same.

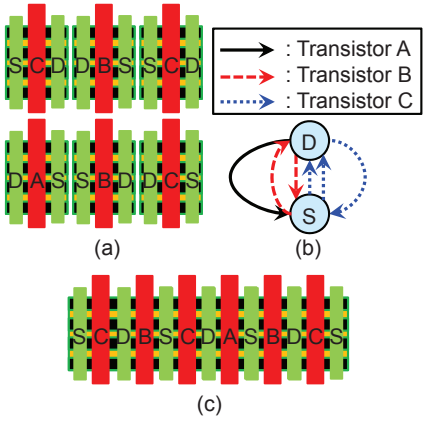

Figure 5: An example of constructing the diffusion graph. (a) A set of sub-transistors with fixed orientation. (b) The corresponding diffusion graph of (a). (c) The generated row placement by searching the diffusion graph in (b).

Once all sub-transistors are assigned into different rows, we should consider the diffusion-sharing for transistors. We construct the diffusion graph of the sub-circuit in each row, and then we find the Euler paths on the diffusion graph [20]. However, the diffusion graph we used in this paper is different from [20]. As described in the previous subsection, we have determined the orientation of all sub-transistors. To avoid degrading the current mismatch, the orientations of all sub-transistors cannot be changed during searching the Euler path. Therefore, the constructed diffusion graph is a directed graph instead of a undirected graph used in [20], where the number of directed edges originated from source node (S) to drain node (D) equals to the number of sub-transistors with drain-side misalignment, and vice versa. For example, given a set of sub-transistors with fixed orientation as shown in Figure 5(a), a directed diffusion graph can be created as given in Figure 5(b). In this example, for simplification, we assume that the source terminal/drain terminal of different sub-transistors can be merged. If the source/drain terminals of some sub-transistors cannot be merged, extra source/drain nodes in the diffusion graph is created.

According to the spatial correlation model in Section 2, to effectively maximize the dispersion degree of a common-centroid FinFET placement, all sub-transistors belonging to the same transistor should be properly separated while the sub-transistors belonging to different transistors should be as close as possible. For clear presentation, we define different kinds of sub-transistors in Definition 1.

DEFINITION 1. *Two sub-transistors are called* **unrelated transistors** *(***related transistors***), if they belong to different transistors, t_i and t_j (the same transistor, t_i).*

To effectively maximize the dispersion degree of a common-centroid FinFET placement, we set a maximum separation (minimum separation) constraint, as defined in Definition 2, for two unrelated transistors (related transistors) to constrain the selection of edge during finding the Euler paths such the dispersion degree can be effectively maximized.

DEFINITION 2. *A* **maximum separation constraint** *(***minimum separation constraint***) is the maximum (minimum) allowable distance between two neighboring unrelated transistors (related transistors) when finding the Euler paths, which is denoted by D_{max_sep} (D_{min_sep}). The distance between two neighboring sub-transistors refers to the number of sub-transistors between the neighboring sub-transistors.*

During searching the Euler path, we only choose the edge satisfying both maximum and minimum separation constraints to properly distribute different sub-transistors while maximizing the dispersion degree. Initially, D_{min_sep} is set to 0 and D_{max_sep} is set to the number of sub-transistors in the row to start the procedure of searching the Euler paths. By iteratively increasing D_{min_sep} and decreasing D_{max_sep} during the procedure of searching the Euler path until an extra diffusion gap is required, the dispersion degree of the resulting row placement can be effectively maximized. After obtaining the Euler paths, the sub-transistors on the same Euler path are merged with diffusion sharing. For example, starting from the source node, as seen in Figure 5(b), an optimized row placement, as shown in Figure 5(c) can be obtained by iteratively searching the Euler paths with decreasing the maximum separation constraint and increasing the minimum separation constraint. In this example, the iteration stops when D_{max_sep} = 3 and D_{min_sep} = 1, which does not incur an extra diffusion gap.

Since the sub-transistors in $(m-i+1)^{th}$ row are symmetrical to that in i^{th} row for a m-row common-centroid FinFET placement, its placement can be derived by placing merged sub-transistors in $(m-i+1)^{th}$ row in the reverse order of that in i^{th} row. By performing the above steps for each row, we can obtain a final

common-centroid FinFET placement such that the diffusion sharing and the dispersion degree among all sub-transistors in each row is maximized.

4.3 Dispersion Degree Maximization

After obtaining an initial common-centroid FinFET placement with optimized diffusion sharing and dispersion degree of the sub-transistors in each row, we further maximize the dispersion degree of sub-transistors in different rows by adjusting the relative positions of different sub-transistors among different rows. We first perform placement rotation for each row by iteratively moving the sub-transistor at the end of the row to the beginning of the row. For example, given a row placement, as shown in Figure 6(a), after iteratively moving the sub-transistor at the end of the row to the beginning of the row, we can derive other three row placements, as shown in Figure 6(b)–(d).

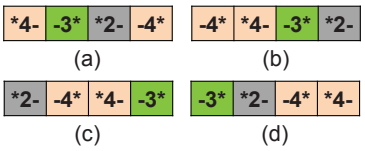

Figure 6: An example of placement rotation in a row. (a) An initial row placement. (b)–(d) Three derived row placements after placement rotation.

After performing placement rotation for each row, we need to determine the best placement of each row with the largest dispersion degree of the sub-transistors in different m rows. The simultaneous selection of the best placement of different rows can be formulated as the shortest path (SP) problem. Initially, a source node (S) and a sink node (T) are created, respectively. For a respective row, a group node is created, where a set of element nodes representing the possible row placements are contained in the group node, as demonstrated in Figure 7. Once the group nodes and element nodes are created, we then add a set of directed edges from S to each element node in the group node corresponding to the first row, and a set of directed edges from each element node in the group node corresponding to the last row to T, where the weight of these edges are all zero.

For two adjacent rows, there is a directed edge from an element node in the group node corresponding to the i^{th} row to an element node in the group node corresponding to the $(i+1)^{th}$ row, where $1 \leq i < m$. The weight of each edge is calculated based on Equation (8), which indicates the current mismatch. By finding the shortest path from S to T, the best placement of each row can be determined and the dispersion degree of the whole common-centroid FinFET placement can be further maximized.

Figure 7 shows an example of the SP formulation for a 4-row common-centroid FinFET placement. Each row has three possible row placements after placement rotation. After solving the SP problem, the 2^{nd}, 1^{st}, 3^{rd}, and 2^{nd} placements of the 1^{st}, 2^{nd}, 3^{rd}, and 4^{th} rows are selected to achieve the best common-centroid FinFET placement with the maximum dispersion degree.

5. EXPERIMENTAL RESULTS

We implemented the proposed common-centroid FinFET placement methodology in the MATLAB programming language on a 3.4GHz Windows machine with 16GB memory. To demonstrate the effectiveness of our approach, we created a set of testcases of current mirrors, CM1, CM2, ..., CM8, with different width ratios of the transistors as shown in the second column of Table 2.

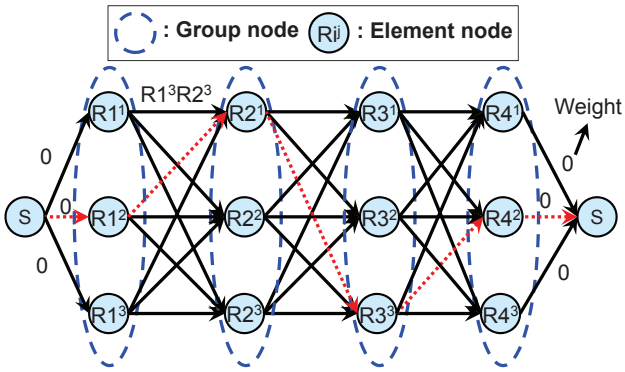

Figure 7: An example of the shortest-path (SP) formulation for a 4-row common-centroid FinFET placement.

We compared our approach with Lin *et al.*'s approach [14], which is known to be the most recent work in the literature handling common-centroid transistor placement with the considerations of diffusion sharing and dispersion. For each common-centroid FinFET placement generated by both approaches, we performed SPICE simulation based on the BSIM-CMG model [15] to obtain the drain current of each transistor in the current mirror. We also evaluate the current mismatch based on Equation (8) and the dispersion degree based on Equation (2).

TABLE 3 show the experimental comparisons of Lin *et al.*'s approach and ours. The results show that our approach results in much better current matching and even better dispersion degree in all test cases. We did not compare the placement area because the area resulting from both approaches for each test case is the same. The runtime based on our approach is longer because we additionally optimize sub-transistor orientations for minimizing the impact of gate misalignment. Consequently, it is very important to consider the impact of gate misalignment and dispersion during common-centroid FinFET placement.

Table 2: Benchmark statistics.

Circuits	# of Sub-transistors
CM1	1, 1
CM2	1, 1, 2
CM3	1, 1, 2, 4
CM4	1, 1, 2, 4, 8
CM5	1, 1, 2, 4, 8, 16
CM6	1, 1, 2, 4, 8, 16, 32
CM7	1, 1, 2, 4, 8, 16, 32, 64
CM8	1, 1 ,2, 4, 8, 16, 32, 64, 128

6. CONCLUSIONS

In this paper, we have introduced the impact of gate misalignment to the drain current of different common-centroid FinFET placements. We have proposed a novel common-centroid FinFET placement approach to generate the common-centroid FinFET placements while considering the impact of gate misalignment and dispersion. Experimental results show that the proposed common-centroid FinFET placement methodology can effectively reduce the

Table 3: Comparisons of simulated current ratios, current mismatch (ϵ), and dispersion degree (L), based on Lin *et al.*'s and our approaches.

Circuits	Lin *et al.*'s approach [14]			Our approach			Comparison (%)	
	Simulated Current Ratio	ϵ / L	Time (s)	Simulated Current Ratio	ϵ / L	Time (s)	ϵ / L	Time
CM1	1 : 0.93	0.07 / 0.90	0.01	1 : 1	0.00 / 0.90	0.01	-100/0.00	0.00
CM2	1 : 1 : 1.85	0.14 / 2.73	0.02	1 : 1 : 2	0.00 / 2.73	0.02	-100/0.00	0.00
CM3	1 : 1 : 1.85 : 3.92	0.22 / 5.55	0.03	1 : 1 : 1.93 : 3.86	0.12 / 5.58	0.04	-46.14/0.61	33.10
CM4	1 : 1 : 1.85 : 3.92 : 4.00	0.35 / 9.19	0.04	1 : 1 : 1.93 : 3.93 : 7.63	0.24 / 9.48	0.05	-30.00/3.18	25.13
CM5	1 : 1 : 1.85 : 3.77 : 8.00 : 15.11	0.41 / 13.69	0.07	1 : 1 : 1.93 : 3.86 : 7.78 : 15.48	0.28 / 14.23	0.11	-32.29/3.94	71.45
CM6	1 : 0.93 : 1.92 : 3.85 : 7.48 : 15.11 : 31.26	0.60 / 19.09	0.20	1 : 1 : 1.93 : 3.93 : 7.63 : 15.33 : 30.89	0.45 / 19.91	0.55	-25.72/4.31	180.87
CM7	1: 1 : 1.85 : 3.85 : 7.92 : 15.63 : 31.11 : 60.95	0.79 / 25.23	0.75	1 : 1 : 1.93 : 3.86 : 7.71 : 15.26 : 30.81 : 61.77	0.48 / 26.36	3.38	-38.83/4.47	351.26
CM8	1 : 0.93 : 1.85 : 3.85 : 7.55 : 15.48 : 31.26 : 61.77 : 122.70	0.93 / 32.13	3.44	1 : 1 : 1.93 : 3.86 : 7.71 : 15.48 : 30.96 : 61.92 : 122.60	0.54 / 33.62	5.10	-41.86/4.63	48.19

impact of gate misalignment to the drain current and maximize the dispersion degree of a common-centroid FinFET placement.

7. REFERENCES

[1] International Technology Roadmap for Semiconductors, 2012.

[2] T. Chiarella, L. Witters, A. Mercha, C. Kerner, M. Rakowski, C. Ortolland, L.-ÃĚ. Ragnarsson, B. Parvais, A. De Keersgieter, S. Kubicek, A. Redolfi, C. Vrancken, S. Brus, A. Lauwers, P. Absil, S. Biesemans, and T. Hoffmann. Benchmarking SOI and bulk FinFET alternatives for PLANAR CMOS scaling succession. *Solid-State Electron.*, 54(9):855–860, Sept. 2010.

[3] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. *Introduction to Algorithms*. MIT Press and McGraw-Hill Book Co., 2 edition, 2001.

[4] R. Dreslinski, M. Wiekowski, D. Blaauw, D. Sylvester, and T. Mudge. Near-threshold computing: reclaiming MooreâĂŹs law through energy efficient integrated circuits. In *Proceedings of the IEEE*, pages 253–266, 2010.

[5] M. Fulde, A. Mercha, C. Gustin, B. Parvais, V. Subramanian, K. von Arnim, F. Bauer, K. Schruefer, D. Schmitt-Landsiedel, and G. Knoblinger. Analog design challenges and trade-offs using emerging materials and devices. In *Proceedings of IEEE European Solid State Device Research Conference*, pages 123–126, 2007.

[6] A. Hastings. *The Art of Analog Layout*. Prentice Hall, 2 edition, 2006.

[7] C.-C. Huang, C.-L. Wey, J.-E. Chen, and P.-W. Luo. Optimal common-centroid-based unit capacitor placements for yield enhancement of switched-capacitor circuits. *ACM T DES AUTOMAT EL*, 19(1):7:1–7:13, Dec. 2013.

[8] Y. Li, Z. Zhang, D. Chua, and Y. Lian. Placement for binary-weighted capacitive array in SAR ADC using multiple weighting methods. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 33(9):1277–1287, Sept. 2014.

[9] C.-W. Lin, C.-L. Lee, J.-M. Lin, and .-J. Chang. Analytical-based approach for capacitor placement with gradient error compensation and device correlation enhancement in analog integrated circuits. In *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pages 635–642, 2012.

[10] C.-W. Lin, J.-M. Lin, Y.-C. Chiu, C.-P. Huang, and S.-J. Chang. Mismatch-aware common-centroid placement for arbitrary-ratio capacitor arrays considering dummy capacitors. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 31(12):1789–1802, Dec. 2012.

[11] M. P.-H. Lin, Y.-T. He, V. W.-H. Hsiao, R.-G. Chang, and S.-Y. Lee. Common-centroid capacitor layout generation considering device matching and parasitic minimization. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 32(7):991–1002, July 2013.

[12] M. P.-H. Lin, V. W.-H. Hsiao, and C.-Y. Lin. Parasitic-aware sizing and detailed routing for binary-weighted capacitors in charge-scaling DAC. In *Proceedings of ACM/IEEE Design Automation Conference*, pages 1–6, 2014.

[13] M. P.-H. Lin, H. Zhang, M. D. F. Wong, and Y.-W. Chang. Thermal-driven analog placement considering device matching. In *Proceedings of ACM/IEEE Design Automation Conference*, pages 593–598, 2009.

[14] M. P.-H. Lin, H. Zhang, M. D. F. Wong, and Y.-W. Chang. Thermal-driven analog placement considering device matching. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 30(3):325–336, Mar. 2011.

[15] W. Liu, X. Jin, J. Chen, M-C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P.K. Ko, and Chenming Hu. Bsim 3v3.2 mosfet model users' manual. Technical Report UCB/ERL M98/51, EECS Department, University of California, Berkeley, 1998.

[16] D. Long, X. Hong, and S. Dong. Optimal two-dimension common centroid layout generation for MOS transistors unit-circuit. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pages 2999–3002, 2005.

[17] P.-W. Luo, J.-E. Chen, C.-L. Wey, L.-C. Cheng, J.-J. Chen, and W.-C. Wu. Impact of capacitance correlation on yield enhancement of mixed-signal/analog integrated circuits. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 27(11):2097–2101, Nov. 2008.

[18] Q. Ma, L. Xiao, Y. C. Tam, and E. F. Y. Young. Simultaneous handling of symmetry, common centroid, and general placement constraints. *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, 30(1):85–95, Jan. 2011.

[19] Q. Ma, E. F. Y. Young, and K. P. Pun. Analog placement with common centroid constraints. In *Proceedings of ACM/IEEE International Conference on Computer-Aided Design*, pages 579–585, 2007.

[20] R. Naiknaware and T.S. Fiez. Automated hierarchical CMOS analog circuit stack generation with intramodule connectivity and matching considerations. *IEEE J. Solid-State Circuits*, 34(3):304–303, Mar. 1999.

[21] S. H. Rasouli, K. Endo, and K. Banerjee. Variability analysis of FinFET-based devices and circuits considering electrical confinement and width quantization. In *Proceedings of IEEE/ACM International Conference on Computer-Aided Design*, pages 505–512, 2009.

[22] B. Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Book Co., 2000.

[23] S. Sarangia, S. Bhushana, A. Santraa, S. Dubeyb, S. Jitb, and P. K. Tiwari. A rigorous simulation based study of gate misalignment effects in gate engineered double-gate (DG) MOSFETs. *Superlattices Microstruct.*, 60(0):263–279, Aug. 2013.

[24] R. Valin, C. Sampedro, M. Aldegunde, A Garcia-Loureiro, N. Seoane, A Godoy, and F. Gamiz. Two-dimensional monte carlo simulation of DGSOI MOSFET misalignment. 59(6):1621–1628, June 2012.

[25] P. Wambacq, B. Verbruggen, K. Scheir, J. Borremans, M. Dehan, D. Linten, V. De Heyn, G. Van der Plas, A Mercha, B. Parvais, C. Gustin, V. Subramanian, N. Collaert, M. Jurczak, and S. Decoutere. The potential of FinFETs for analog and RF circuit applications. *IEEE Trans. Circuits Syst. Regul. Pap.*, 54(11):2541–2551, Nov. 2007.

[26] L. Xiao and E. F. Y. Young. Analog placement with common centroid and 1-D symmetry constraints. In *Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference*, pages 353–360, 2009.

[27] T Yan, S. Nakatake, and T. Nojima. Formulating the empirical strategies in module generation of analog MOS layout. In *Proceedings of the IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures*, pages 44–49, 2006.

[28] L. Zhang, S. Dong, Y. Ma, and X. Hong. Multi-stage analog placement with various constraints. In *Proceedings of IEEE International Conference on Communications, Circuits and Systems*, pages 881–885, 2010.